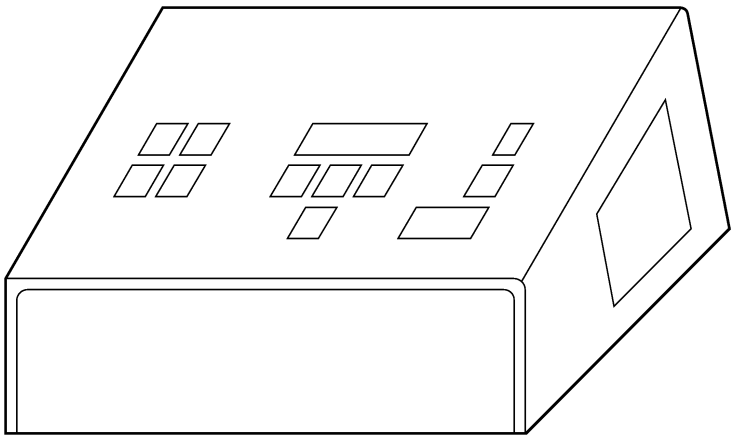
durst

AF 2000
Service manual

2.1



Notice

This service manual has been edited in June 1992;
the first unit name ELITE 2000 has been re-named in
AF 2000.

This is the revised manual version **2.1 edited in May 1999 (updated circuit diagrams, corrected errors)**

Utmost care was taken to ensure a flawless manual; we are, however, most grateful for all suggestions for improvement or correction.

For your suggestions please use the enclosed reply letter.

The service manual order code number is: **SM00550**

REPLY LETTER

We' d like to receive your comments on this repair manual. Please answer the questions and return this form to:

Durst Phototechnik AG, att. service department.

Service manual for unit: _____

❑ 1. Version ❑ 2. Version ❑ 3. Version ____ Version

Have you found any mistakes? Which?

_____

_____

_____

Did this manual help you to find an error cause?

_____

_____

_____

What was the mistake?

_____

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What was the solution?

_____

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Have you suggestions concerning the completion of the manual? Which topics should be added?

_____

_____

_____

SUMMARY

DIAGRAMS

1.1 GENERAL DESCRIPTIONS

DURST ELITE 2000 - is a microprocessor-controlled autofocus System for Durst M 805 and L 1200 enlarger models

Technical data

Lens carrier adjustment speed:	fast = approx. 6.5 mm/sec. slow = approx. 0.5 mm/sec.
Programmable lens focal lengths:	from 35 up to 250 mm
Resolution of positioning device:	0.01 mm
Repeatability of lens setting:	± 0.02 mm
Enviromental conditions:	30 - 80 % relative humidity 18 - 30 degrees centigrade
Lens Channels:	10 (0 - 9)
Positive variator range:	+ 999 / - 99 mm
Negative variator range:	+ 99 / - 99

For M 805 ELITE

Exposure timer range:	0 - 99.9 100-999 sec.
Lens aperture range:	F/STOP 2.8 - 45

This service manual can be used for following variants:

Elite 2000 TIM	autofocus control with timer
Elite 2000	autofocus control without timer
Elite 2000 MOT	autofocus control with motorized head movement control

On principle, they are interchangeable with regard to the automatic focusing function.

The main difference between the control desks lies in the number of keys on the keyboard, position of Jumper S 1 on the power control board and soldering bridge "M 805" on the keyboard.

The "MOT" version boasts an additional transformer, a 24 V_ motor control board and an interface PCB.

For functional description of the motor control, see D.1.
For troubleshooting aid, see C.0.2

1. Elite 2000 TIM

   Processor keyboard PCB:

   - keys S 11, 12, 13 are not mounted
   - soldering bridge closed
   - S 1 is open

2. Elite 2000

   Processor keyboard PCB:

   - keys S 11, 12, 13 are not mounted
   - soldering bridge open
   - S 1 is open

3. Elite 2000 MOT

   Processor keyboard PCB:

   - keys S 11, 12, 13 are mounted
   - soldering bridge open
   - S 1 is closed

Operational description

The system consists of the Elite 2000 Control desk and the AF module.

The AF module is identical for all variants.

The system uses a potentiometer for feedback information about the colorheads vertical position.

The potentiometer resistance determines the duty cycle of monoflop V 6 on the power control interface PCB.

During this duty cycle (3 - 6 msec.) pulses of 1.2 MHz frequency are counted into binary counters V 16 and V 18. The duration of the duty cycle varies with the colorhead's height and thereby the number of pulses counted by V 16 and V 18.

Thus A/D conversion takes place.

The microprocessor calculates the necessary lens displacement according to the programmed values. It activates the lens motor thru V 13, V 14 (interface PCb) and V 2, V 1 on the lens motor PCB.

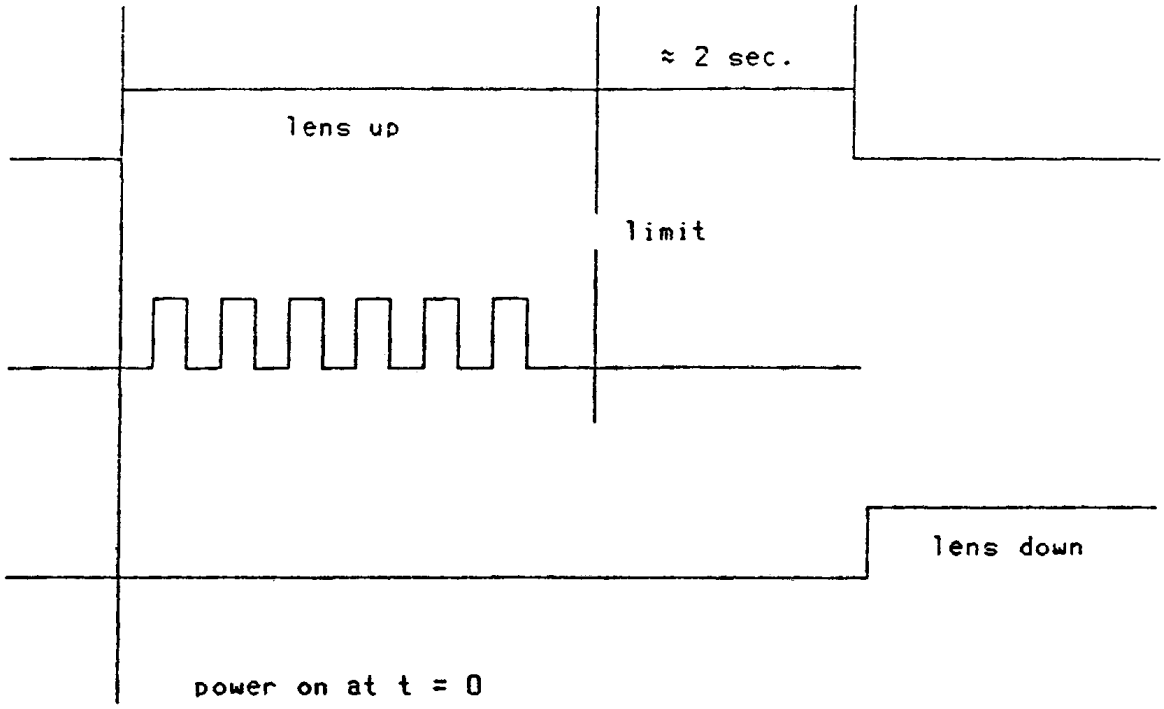
The lens motor is a 30 V DC motor. Thus a feedback becomes necessary, as to determine the real lens displacement.

An optical disk in connection with an optosensor (V 9) supplies the necessary pulses via V 2, V 7 to the power control PCB.

The microprocessor switches the pulses via the nand-gates V 15 to binary counters V 16 and V 18.

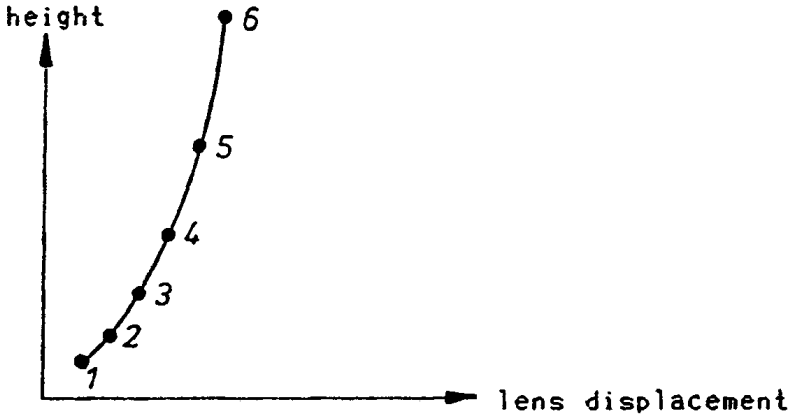
The lens reference position is determined after power on. The lens motor is activated and pulls the lens standard up to the stop position. Once the limit is reached, the optical disk stops supplying pulses. The microprocessor waits for approx. 2 seconds. If no pulses occur during this lapse, the position is taken for the upper 1ens limit position = reference position.

The microprocessor fetches the programming values, the potentiometer limit values from the register and polls counters V 16, V 18 (for actual colorhead position) to determine the necessary lens displacement.



The programming values are determined during a programming session performed by the operator. The operator selects a cannel and focuses the lens manually at 5 or 6 different head positions.

The microprocessor stores the number of pulses which occur during each focussing operation. Once the session is over, all intermediate points are approximated by a curve.



Note:

The head limit positions are stored in two registers inside the ram.

If the contents of the registers are lost, reprogramming becomes necessary (Refer to 2.4).

Otherwise the unit cannot be operated!!!

Error messages:

Err. 7 - Error in the autofocus system
- Pulses missing
- Pulse sequence to slow

Err. 6 - Bad program values

* Z 80 + ENVIRONMENT

The microprocessor receives its instructions from eprom V 6.

When power is applied to the system, V 22 on the power control interface PCB provides the 5 VDC supply voltage and a reset-signal. Once the reset signal goes to H, the processor starts operating.

The first operation is to fetch the first instruction contained in V 6. Therefore the read output goes to L, while V 5 is activated thru a MREQ signal.

V 5 decodes the inputs (A, B, C all L) and outputs Y0 goes L. Thereby eprom V 6 is enabled and delivers the data word contained in address 0000. The data word can be 1, 2 or 3 bytes long.

When a data word must be memorized, the WR output goes to L. The ram (V 7) is selected via address 4000 to 4FFF, and the data word present on the data inputs is memorized in the ram.

The data is retrieved when the processor puts out the correct address and the read output goes to L level.

The keyboard is selected via V 11. When pins 1 and 15 are at L level, this IC transfers the logic level at the "A" inputs to the "Y" outputs. The keyboard is a matrix-circuit.

The microprocessor selects one row of keys by supplying an appropriate address word.

When a key is pressed the corresponding line is pulled to 1 level.

V 11 transfers this logic state to the data bus, the microprocessor can "read" which key has been pressed.

V 12, V 28, V 29 form a multiplexing circuit to switch on one display or led-row at a time.

V 10 selects either keyboard, display or interface devices on the power control interface PCB.

Address pages:

I/O	address	part
I	0000-3FFF	eprom
I/O	4000-47FF	ram
O	C000	interrupt reset
O	8000	display multiplexer V 12
O	8004	display high
O	8008	display low
I	8000	any key
I	8006	key-row 0 (S 10, 11, 12 ...)
I	8005	key-row 1 (S 6, 7, 8 ...)
I	8003	key-row 2 (S 1, 2, 3 ...)

POWER CONTROL PCB

Address pages:

I/O	address	port
I	8010	V 19
I	8020	V 17
O	800C	V 14

data	output structure for V 14						
D 0	D 1	D 2	D 3	D 4	D 5	D 6	D 7
if 0: count lens pulse if 1: A/D conversion	if 0: reset counters and trigger monoflop V 6	if 1: relay on	if 1: lens up	if 1: lens down	if 1: head up	if 1: head down	if 1: rapid

2.2 SOLID STATE DEVICES

Microcomputer and TTL

- Z 80 CPU
- 27128 eprom
- 5517 TC ram
- TIMER 555
- 74 LS 138
- 74 LS 139
- 74 LS 175
- 74 HCT 244
- 74 LS 244
- 74 LS 273
- 74 LS 374
- 74 LS 393

CMOS

- 4016
- 4070
- 4098

OPAMPS

- LM 339
- LM 324

STABILIZERS

- L 296
- 7812

DISCRETE

- BC 237
- BC 337
- BC 327
- IRF 532 (BUZ 20)
- TIP 147

SPECIAL

- L 298

General explanation of terms:

H: Logic high

L: Logic low

Maximum input low:

This is the highest input voltage that the device will recognize as a low level. A higher voltage might be interpreted as high, or low. It is not defined.

Minimum input high:

This is the minimum voltage required. So the device will recognize the level as being high. A lower voltage is not defined.

Maximum output low:

The manufacturer guarantees that the device will not deliver a voltage lower than this if the output is at L level.

Minimum output high:

The device will deliver a voltage which is not lower than this value, if the output is at H level.

Z 80 CPU

The Z 80 central processing unit is 8 bit microprocessor which may run on 2.5 MHz to 8 MHz clocks.

Operation is possible with supply voltage 4.74 V ≤ VCC ≤ 5.25 V.

Operating temperature range is 0° to 70° C.

Maximum input low: 0.8 V
" " high: 7 V

Minimum input low: - 0.7 VCC
" " high: 2 VCC

Maximum output low: 0.4 V
Minimum " high: 2.4 V

All outputs can either be high, low or high impedance.

The Z 80 CPU is capable of arithmethic, logic and I/O operations.
The CPU accepts 2 interrupt input signals:

- NMI (non maskable interrupt)
- INT

The NMI has first priority.

The INT input has lower priority and its acknowledgement must be enabled thru an instruction in the software.

The NMI cannot be disabled thru software.

After detection of the NMI input signal (pin 17 goes L) the CPU jumps to 0066 (H).

The INT input is acknowledged only if the bus req input is not active.

A 0 - A 15 ADDRESS BUS

The 16 bit address bus supplies the addresses for selecting I/O ports and memory locations in the rams / eproms.

Each I/O port is selected by an address combined with a read or write signal. Thus the CPU is enabled to read or write data from external devices like sensors, counters and activate motors.

D 0 - D 7 DATA BUS

The 8 data inputs / outputs are used for data exchanges with memory devices (ram, eproms) and I/O ports.

M 1 MACHINE CYCLE ONE

This output carries information:

If M 1 is active together with MREQ (both active L), it indicates that during the current cycle the opcode is fetched.

If M 1 is active together with the IORQ output, the CPU has acknowledged an interrupt signal.

RESET (input, active low)

The reset input initializes the CPU, clears all registers.

While the reset input is L, the address and data bus go to high impedance.

WR
--

When the write output goes to L state, the CPU data bus holds valid data to be stored at the memory location or I/O port indicated on the address bus.

Manufacturers:

- Zilog
- Mostek
- Toshiba
- SGS

27128

The 27128 is an UV erasable electrically programmable memories with

16 KByte storage = 128 Kbits

Operating temperature range:	0° - 70 70°C		
Power supply VCC:	5 V ± 0.25		
Input L voltage:	min.	- 0.1	V
	max.	.0.8	V
Input H voltage:	min.	2	V
	max.	5.7	V
Output L voltage:	max.	0.45	V
Output H voltage:	min.	2.4	V
Maximum active current:	125 mA		
Maximum standby current:	30 mA		

ERASURE

Erasure occurs when the window is exposed to wavelengths shorter than 4000 A.

Sunlight and certain fluorescent lights can erase the eprom.

The opaque label should be left in place.

DEVICE OPERATION

Read

The 27128 has two control inputs: OE and CE. Both must be active (L) to obtain data at the outputs.

STANDBY

When the CE input is H, the 27128 goes to standby mode independent of the OE input.

The max. current consumption falls to less than 40 mA.

5517

The 5517 is a 2 KByte random access memory. Each byte contains 8 bits.

The 5517 has 2 control inputs: CE and OE.

Both must be active (L) to access the memory. When the CE input is H, the memory switches to standby mode and current consumption drops to 1 micro ampere.

OPERATION	R/W	OE	CE
Read	H	L	L
Write	L	H	L
Standby	X	X	H

The 5517 is pin compatible with the TMR2016P (Texax Instruments).

Power supply voltage VCC: 4.5 to 5.5 V

Input High: 2.2 " 5.3 V

Input Low: - 0.3 " 0.8 V

Data retention voltage: 2 < VCC < 5.5

Manufacturer: Toshiba

NE 555: Timing circuit

is compatible with: MC 1455/1555 (Motorola)
SE 555

Uses an external resistor - capacitor network as timing controllers. Both monostable and astable operation are possible. The output timing is independent of the supply voltage.

Monostable mode (see circuit diagram)

On the interface PCB the 555 is used as one-shot circuit with variable duty cycle. The trigger signal is provided by the CPU via V 14. When pin 2 is at H level, capacitor C 5 is short circuited by an internal transistor. Once the level at pin 2 drops below 1/3 VCC, the 555 is triggered.

The internal transistor is disabled.

Output pin 3 goes to H level. C 5 can charge up at an exponential rate thru R 6 and the factor potentiometer.

Once it reaches 2/3 of VCC, the circuit resets itself and pin 3 returns to L level.

RATINGS	min.	max.
Supply voltage (VCC)	4.5	18
Output L		0.5
Output H	3	
Highest trigger voltage		1/3 VCC

Manufacturers:

- National
- Texas Instruments
- Fairchild

74LS138: Decoder / Multiplexer

RATINGS:

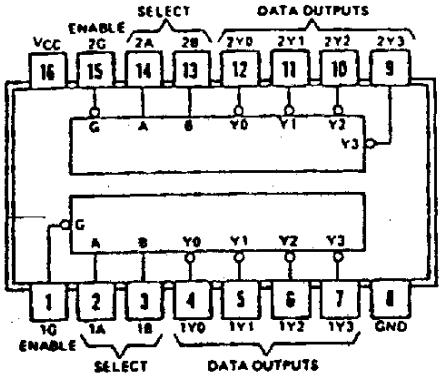
Typical power dissipation:	32 mW
Supply voltage:	4.5 - 5.5 V
Operating air temperature:	0 - 70°C
High level input voltage:	min.: 2 V
Low " " "	max.: 0.8 V
High level output voltage:	min.: 2.7 V
Low " " "	max.: 0.4 V
Absolute max.-supply voltage:	7 V
" " input "	5.5 V

TRUTH TABLE

Inputs				Outputs					
Enable			Address						
G1	G2A	G2B	CBA	Y0	Y1	Y2	Y3	Y4	Y5
X	X	H	X X X	H	H	H	H	H	H
L	X	X	X X X	H	H	H	H	H	H
X	H	X	X X X	H	H	H	H	H	H
H	L	L	L L L	L	H	H	H	H	H
H	L	L	L L H	H	L	H	H	H	H
H	L	L	L H L	H	H	L	H	H	H
H	L	L	L H H	H	H	H	L	H	H
H	L	L	H L L	H	H	H	H	L	H
H	L	L	H L H	H	H	H	H	H	L

74LS139

This IC contains two fully independent 2 to 4 line decoders / multiplexers.



Electrical characteristics

Typical power dissipation: 34 mW

Parameter	Test conditions		SN74LS139A min.	typ	max.	Unit
VIH high level input voltage			2			V
VIL low level input voltage					0.8	V
VOH high level output voltage	VCC=min. VIH=2 V VIL=VIL max. IOH=-400 µA		2.7	3.4		V
VOL low level output voltage	VCC=min. VIH=2 V VIL=VIL max.	IOL=4 mA IOL=8 mA		0.25 0.35	0.4 0.5	V
II Input current at max input voltage	VCC=max. VI=7 V				0.1	mA
IIH High level input current	VCC=max. VI=2.7 V				20	µA
IIL Low level input current	VCC=max. VI=0.4 V				-0.4	mA
IOS Short circuit output current §	VCC=max.	LS139A	-20		-100	mA
IOS Supply current	VCC=max. Outputs enabled and open	LS139A		6.8	11	mA

LS139A
(EACH DECODER/DEMULTIPLEXER)

FUNCTION TABLE

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

74LS244: 2 x 4 buffers with tree-state outputs

The 2 fully indipendent, noninverting buffers have each:

- 1 enable input (L acitve)
- 4 inputs (L or H)
- 4 outputs (three-state)

RATINGS:

Supply voltage:	4.75 - 5.25 V
Temperature range:	0 - 70°C
High level input voltage:	min. 2 V
Low " " "	max. 0.8 V
High level output voltage:	min. 2 V
Low " " "	max. 0.55 V

74LS175

Contains 4 D flip-flops.

Each FF is edge-triggered by the same clock signal.

The level at the "data" input is transferred to the output upon the rising edge of the clock signal.

The output remains at this level until new data is transferred with a clock signal or until the "MR" (master reset) input is activated.

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	MR	CP	DN	QN	$\overline{QN}$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	H	H	L
Load "0"	L	↑	L	L	H

Note that each FF has 2 outputs, with complementary status.

ELECTRICAL CHARACTERISTICS

VOH:	Min. high level output voltage:	2.5	
VOL:	Max. low " " "	0.5	
IN:	" input current (VIN = 7 V):	1	mA
IH:	Max. high level input current:	0.1	mA
IL:	Max. low " " "	- 2	mA

74LS273: Eight D flip-flops

FUNCTION:

The level at the D input is transferred to the Q output on the rising edge of the clock input.

When the clock is at either H or L, the D input has no influence on the Q output

The clear input resets all the Q outputs to L level.

TRUTH TABLE

Clear	Clock	Di	Qi
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H	X	NO CHANGE

RATINGS:

Supply voltage:	4.5 - 5.5 V
Temperature range:	0 - 70°C
High level input:	min. 2 V
Low " "	max. 0.8 V
High level output:	min. 2.4 V
Low " "	max. 0.4 V

74LS393: 2 x 4 bit binary counters

The 73LS393 frequency dividers / counters contain 2 indipendent counters which can be cascaded. Each has a clear (active H) and a clock input.

The output changes on the negative-going edge of the clock input.
A frequency at the clock input is divided by:

				if cascaded			
2	4	8	16	32	64	128	256
QA	QB	QC	QD	QA	QB	QC	QD

74HCT244: CMOS non-inverting octal 3-state line driver

The pinout is identical with the 74LS244.

TRUTH TABLE

G	In	OUTn
H	X	HighZ
L	L	L
L	H	H

ELECTRICAL CHARACTERISTICS

VIH	Min. high level input:	3.2	V
VIL	Max. low " "	1	V
VOH	Min. high " output:	3.7	V
VOL	Max. low " "	0.4	V

74LS374: 8 D-latches

ELECTRICAL CHARACTERISTICS

parameter	test conditions		SN74LS min.	typ.	max.	unit
VIH high level input V			2			V
VIL low level input V			2		0.8	V
VOH high level output V	VCC=min. VIH=2V VIL=VILmax. IOH=max.		2.4	3.1		V
VOL low level output V	VCC=min. VIH=2V VIL=VILmax. IOH=max.	IOL=12mA IOL=24mA		0.25 0.35	0.4 0.5	V
IOZH off-state output current, high level voltage applied	VCC=max. VIH=2V VO=2.7V				20	µA
ICC supply current	VCC=max. Output control at 4.5 V			24 27	40 40	mA

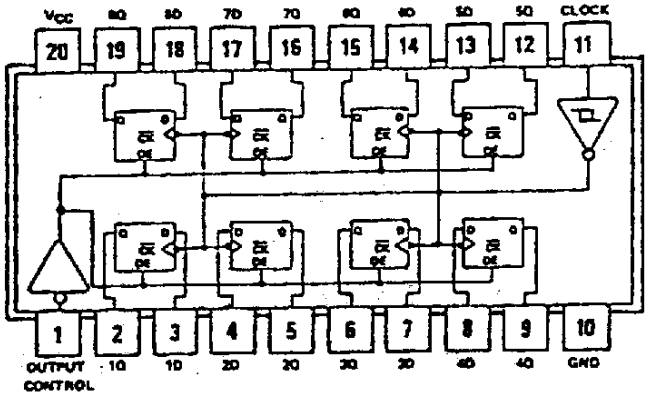
Description

The eight flip-flops of the LS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

Due to Schmitt-trigger buffered inputs at the enable/clock lines noice rejection is typically 400 mV. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z



4016: bilateral switches

These C-MOS switches can transmit analor or digital signals.

Each package contains 4 switches.

The on/off state is controlled by a digital signal at the control inputs.

A H level turns the switch on, 1 L level turns it off.

Max. "ON" resistance at VDD = 10 V is 600 Ω

4070B: quad ex-or gates

TRUTH TABLE

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

ELECTRICAL CHARACTERISTICS: (for VDD = 10 V)

Output voltage: max. L level: 0.05 V
" " min. H " 9.95 V

Input voltage: max. L level: 3 V
" " min. H " 7 V

4098: dual monostable multivibrator (monoflop)

Provides one shot retriggerable operation.

If retriggering during the active period is not desired, $\bar{Q}$ can be tied to TR- or Q to TR+ depending it leading or trailing edge triggering is used.

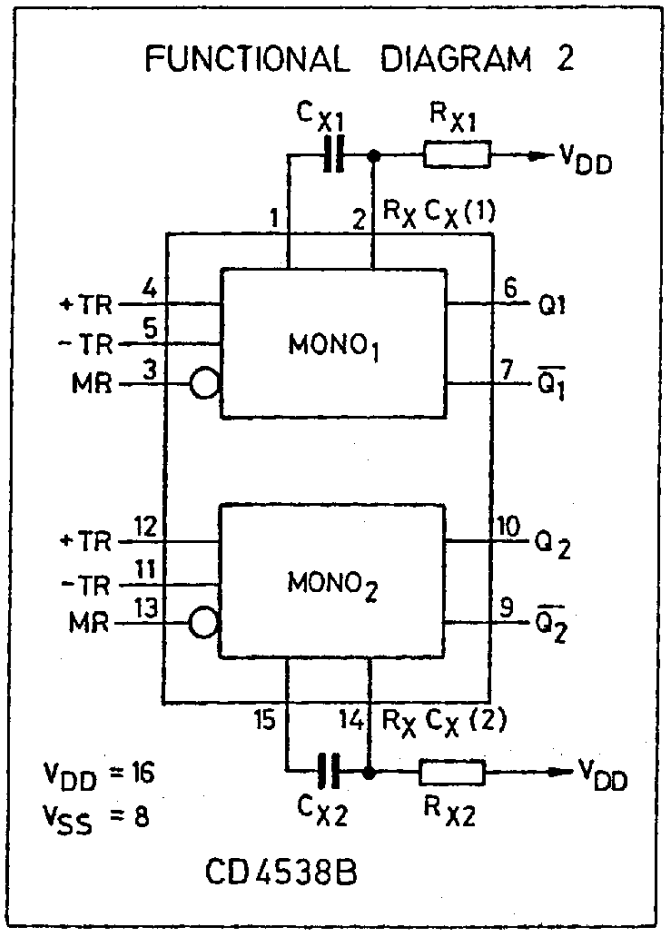
The active period can be calculated as follows: 1/2 R x C

PIN DESCRIPTION

RX, CX
External resistor R and capacitor C determine the active period.

TR
TR+ and TR- start the monoflop.

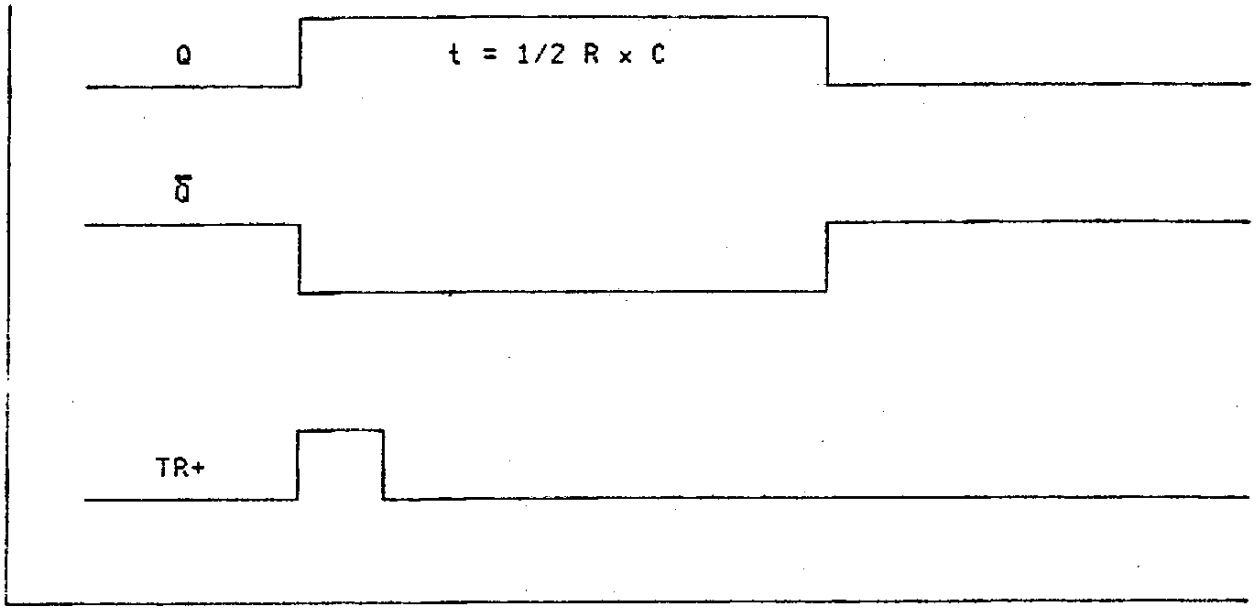
TR+ is used if leading edge triggering is desired
TR- " " " trailing " " " " "



MR
A low level at this input immediately resets the monoflop.

Q
This output is H during the active period and returns to L after the period has finished.

$\overline{Q}$
This output is L during the active period and returns to H after the period has finished.



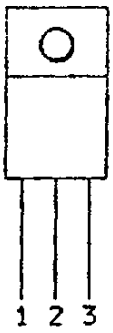
LM324: Quad operational amplifiers

Replacements: MC1741, MC3503, MC3403

Features:

Short circuit protected output
Max. supply voltage: 36 V
4 amplifiers per package
± 13 V output swing

7805 / 7808 / 7812: Three terminal positive voltage regulators



1 = input
2 = ground
3 = output

7805 - 5 V regulator
7808 - 8 V "
7812 - 12 V "

Types with different current capability are available. Some can supply up to 2 A continuous output current.

The regulators are short circuit and heat protected.

CURRENT CAPABILITIS:

Type:	max. continuous current:
78M05 / M08 / M12	0.5 A
7805T / 08T / 12T	1 A
78S05 / S08 / S12	2 A

The regulators do not require any external components for voltage regulation.

The fixed output voltage can vary from one to the other IC: following are typical dispensions:

7805	4.3	to	5.2 V
7808	7.7	"	8.3 V
7812	11.5	"	12.5 V

The regulator keeps this voltage pretty much constant over a wide range of load variations.

Type	AV	load variation	line variation
7805	50 mV (max)	5 to 500 mA	7 - 30 V
7808	80 mV (max)	5 to 500 mA	10 - 30 V
7812	120 mV (max)	5 to 500 mA	14 - 30 V

BC237B: silicon NPN small signal transistor

MAX. RATINGS

VCBO	50	V
VCEO	45	V
VBE	6	V
IC	100	mA
PTOT	0.3	W

ELECTRICAL CHARACTERISTICS

hFE 200 - 500 (IC = 2 mA, VCE = 5 V)

Replacements: BC182, BC107

BC307: PNP silicon transistor

For ratings see BC237.

Replacements: BC161B, BC177

BC338: NPN silicon transistor

MAX. RATINGS

VCBO:	30	V
VCEO:	25	V
VEBO:	5	V
IC:	0.8	A
PTOT:	0.625	W

ELECTRICAL CHARACTERISTICS

hFE: 100 - 600 (IC 100 mA)

VCE (SAT): 0.7 V

Replacements: BC337, BC239

BC327: PNP transistor

Max. collector-emitter voltage (VBE = 0):	50	V
Max. continuous collector current:	0.5	A
Max. base current:	0.1	A
hFE:	100 - 600	

BC327 can be replace by BC297.

THE IRF532: Power MOS field-effect transistor

Is a n-channel enhancement MOS transistor.

Replacements: BUZ 20, RFP12N10 (RCA)

ELECTRICAL CHARACTERISTICS

Drain source breakdown voltage:	100	V
VGS Fhreshold:	2 - 4	V
ID (ON):	12	A
gfs:	5.5	Siemens (typ)
vds (ON):	0.1Ω	Ω
Max power diss.:	75	W

TIP147: Epitaxial PNP power Darlington transistor

ELECTRICAL CHARACTERISTICS - (MAX. RATINGS:)

VCEO:	100	V
VEBO:	5	V
ICM:	20	A
IB:	0.5	A
PTOT:	125	W

OPERATING CHARACTERISTICS

VCE at IC = 30 mA:	100	V
VBE at IC = 10 A, VCE = 4 V:	3	V
hFE at IC = 10 A, VCE = 4 V:	500	

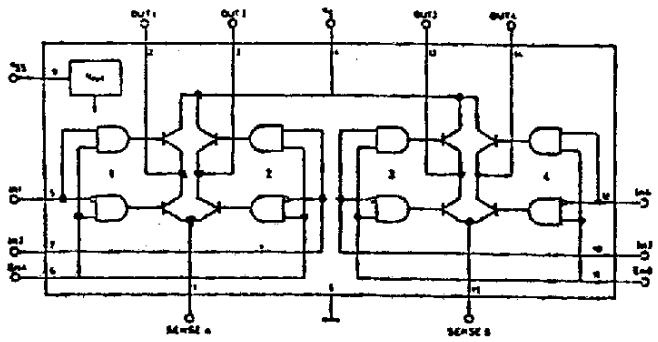
Replacements: BDV64B

L298: Dual full-bridge driver

ABSOLUTE MAX. RATINGS

VS	Power supply:	50 V
VSS	Logic supply voltage:	7 V
IO	Peak output current:	
	non repetive:	3 A
	DC:	2 A

BLOCK DIAGRAM



Manufacturers:

- SGS
- Unitrode

L296: Switching regulator

RATINGS

Max. input voltage:	50	V
Max. voltage at pins: 1, 12	10	V
6, 15	15	V
4, 5, 7, 9	5.5	V
10, 6	7	V

If these limits are exceeded, the circuit will be damaged.

FUNCTION

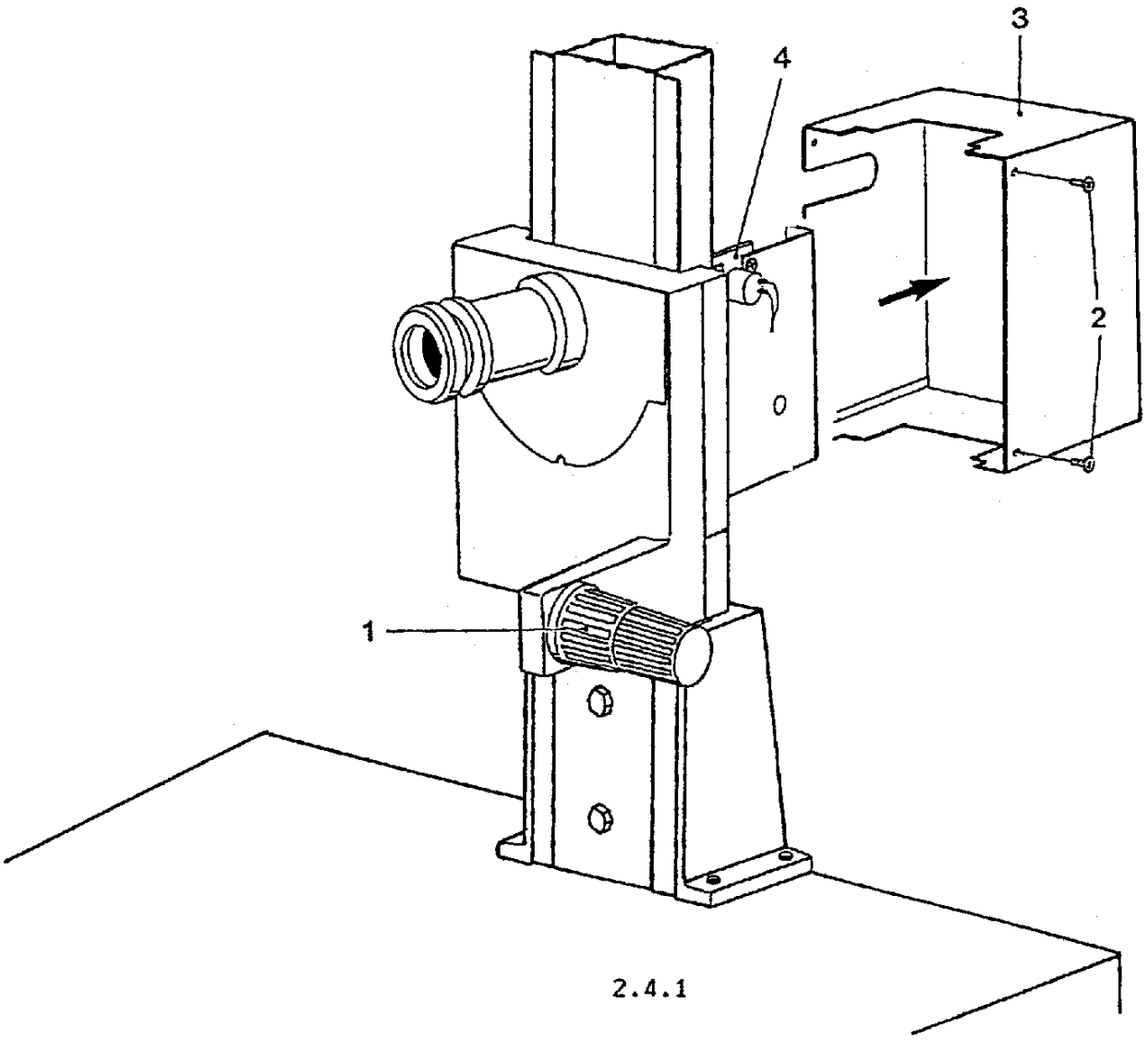
The circuit is internally over-load protected.
The capacitor at pin 5 determines the soft start delay.
The capacitor at pin 13 determines the reset delay.
The reset output stays at L level after power on, the time depends on the capacitor at pin 13.

Manufacturer: SGS

2.4 FACTOR POTENTIOMETER: REPLACEMENT AND CALIBRATION

REPLACEMENT:

1. Move head to lowest position
2. Block head with friction grip (1)
3. Remove screws (2) and cover (3)
4. Remove potentiometer support plate (4)
5. Install new pot on support plate. Turn axle clockwise to stop
6. Turn axle counterclockwise for 1/2 revolution
7. Install in reverse order



Electronical

Action	Purpose
1. Press and hold the enter key. Power up.	Entry into testprogram.
2. Press enter.	Exit from keyboard test: The unit displays a number except 0.
3. Press the AF setup and enter keys simultaneously.	Entry into factor calibration procedure. The "NV" led turns on.
4. Move head to lowest position. Press enter.	Lowest head positon value is stored. "PV" led turns on: "NV" led turns off.
5. Move head to highest position. Press enter.	Highest head positon value is stored. The "PV" led turns off.
6. Power off to exit.	

This procedure initializes the head limit position registers.

The potentiometer values in highest and lowest head position are stored in the ram. This obviates a precise mechanical adjustment.

3.2 TESTPROGRAM

ENTRY INTO TESTPROGRAM

1. Press and hold the enter key. 2. Power on.
3. All leds, displays are switched on for 1.5 sec.

correct — N → Go to 3.A.1.

Y

Keyboard test.

Press each key except the "enter" key.

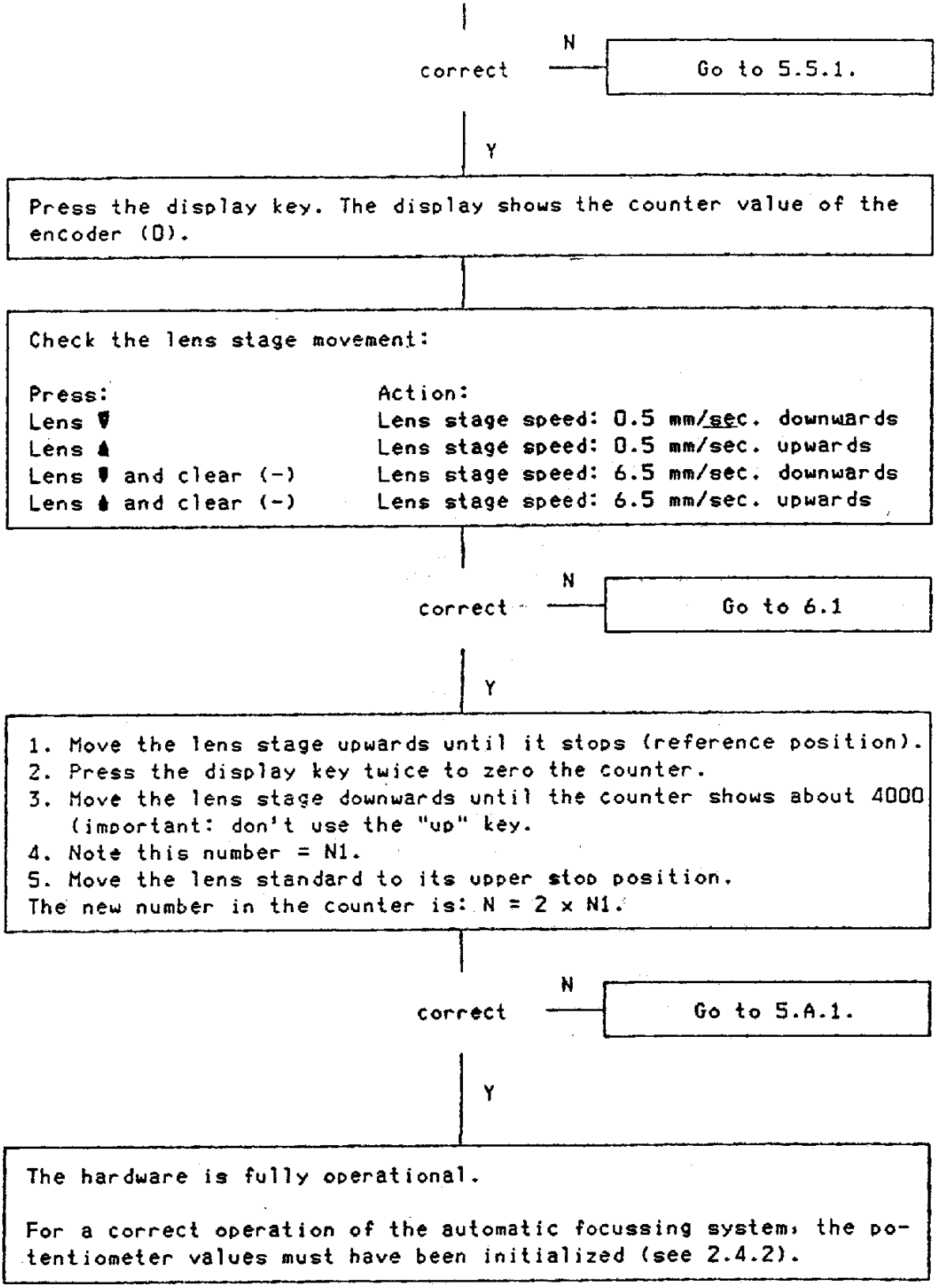
display select	016	
lens up	008	
lens down	004	
AF-setup	002	
-	080	
+	072	
lens channel	068	
expose	066	**
light	144	**
head down	136	*
rapid	132	*
head up	130	*

** only on Elite 2000 TIM
* only on Elite 2000 MOT

correct — N → Go to 3.B.

Y

Press the enter key. The display shows the factor value.
Move head to lowest position: 1300.
Move head to highest position: 10300 (The unit displays 300)
(Tolerance: ± 20%)


correct
N
Go to 5.5.1.
Y
Press the display key. The display shows the counter value of the encoder (D).
Check the lens stage movement:
Press: Action:
Lens ▼ Lens stage speed: 0.5 mm/sec. downwards
Lens ▲ Lens stage speed: 0.5 mm/sec. upwards
Lens ▼ and clear (-) Lens stage speed: 6.5 mm/sec. downwards
Lens ▲ and clear (-) Lens stage speed: 6.5 mm/sec. upwards
correct
N
Go to 6.1
Y
1. Move the lens stage upwards until it stops (reference position).
2. Press the display key twice to zero the counter.
3. Move the lens stage downwards until the counter shows about 4000 (important: don't use the "up" key.
4. Note this number = N1.
5. Move the lens standard to its upper stop position.
The new number in the counter is: N = 2 x N1.
correct
N
Go to 5.A.1.
Y
The hardware is fully operational.
For a correct operation of the automatic focussing system, the potentiometer values must have been initialized (see 2.4.2).

3.3 CONTINUOUS TESTPROGRAM

CONTINUOUS TESTPROGRAM A:

1. Press enter.
2. Press the "up" and "down" keys simultaneously.
3. Lens stage moves down for 30 mm. Stops. Moves up to ref. position.

CONTINUOUS TESTPROGRAM B:

1. Power off to exit testprogram A.
2. Power on with enter key pressed.
3. Move head to the first focussing position of channel 0.
   Press "lens up" + "displ. select".
4. If channel 0 is programmed, and the potentiometer has been calibrated, the lens stage focusses as follows:

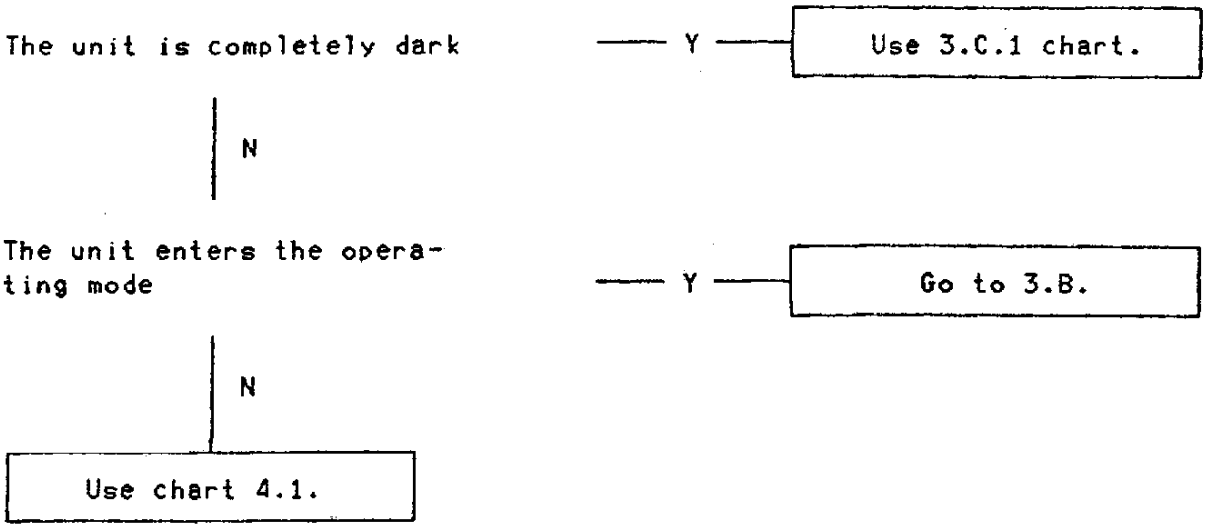
9 times random position	1 time focus position.

CONTINUOUS TESTPROGRAM C: (with ELITE 2000 MOT only)

1. Power off to exit testprogram B.
2. Power on with enter key pressed.
3. Press the "Rapid" and "Light" keys.

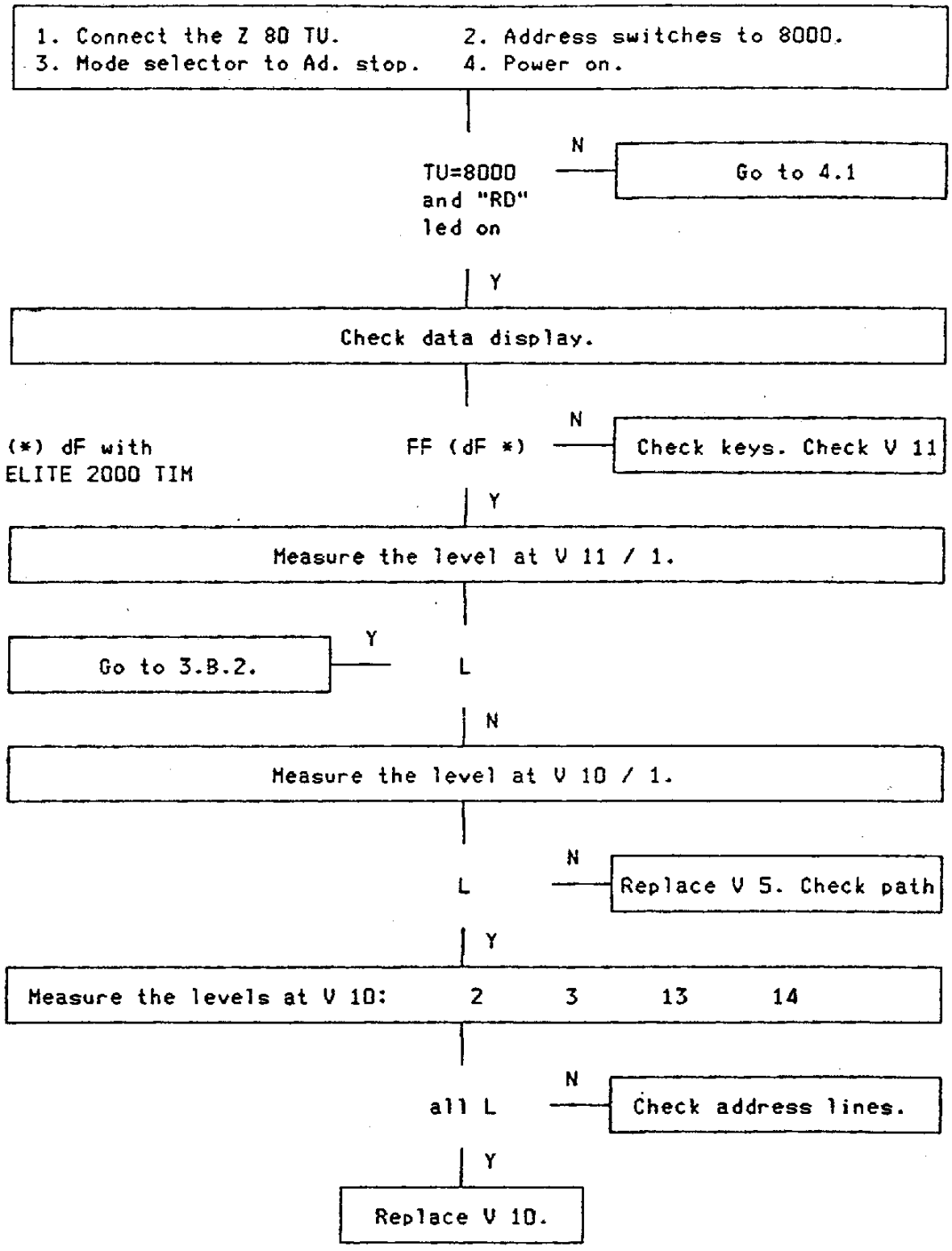
The head moves to upper and lower limit.
The lens moves from reference to 100 mm extension and back.

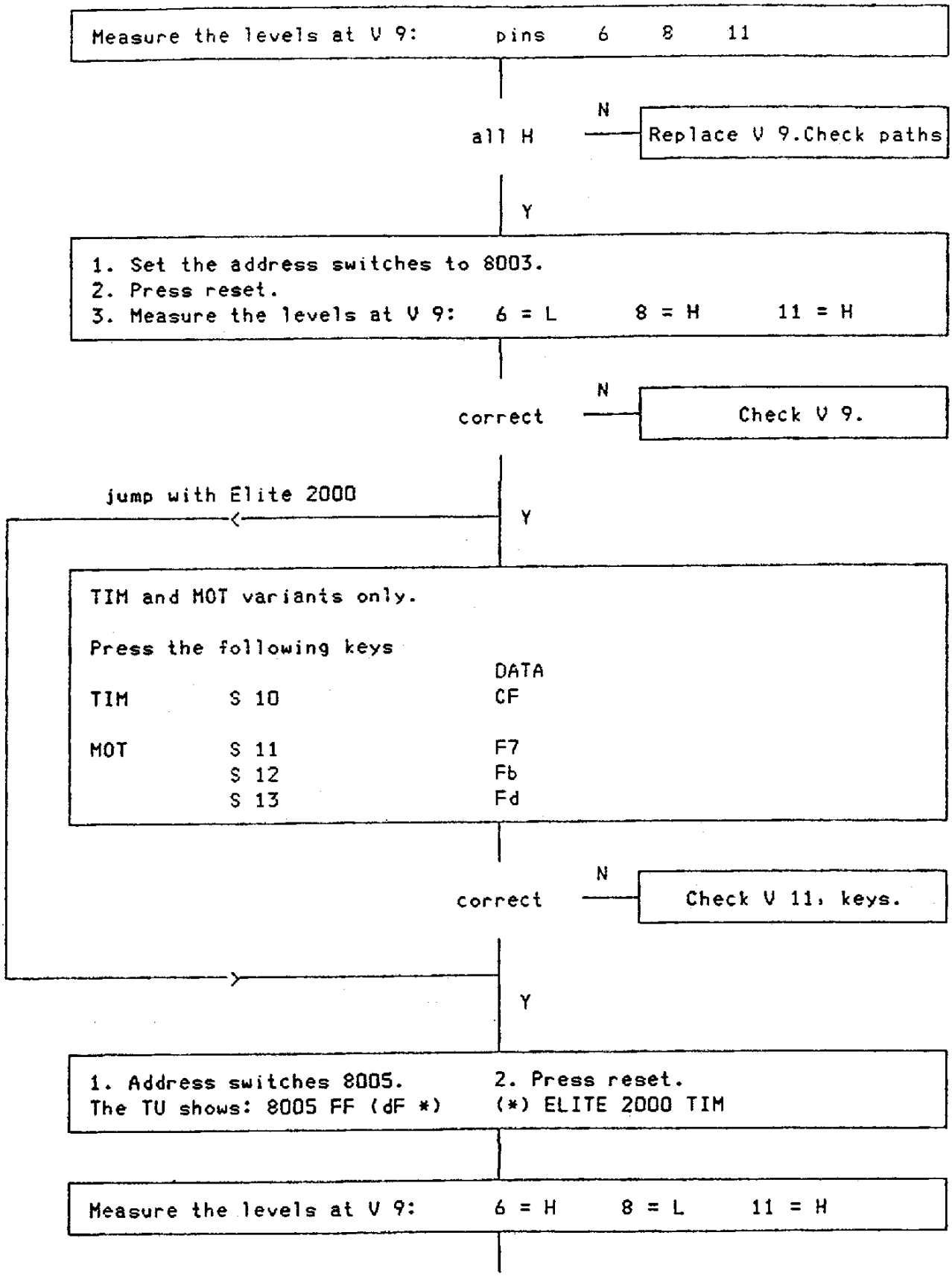
3.A FLOWCHART

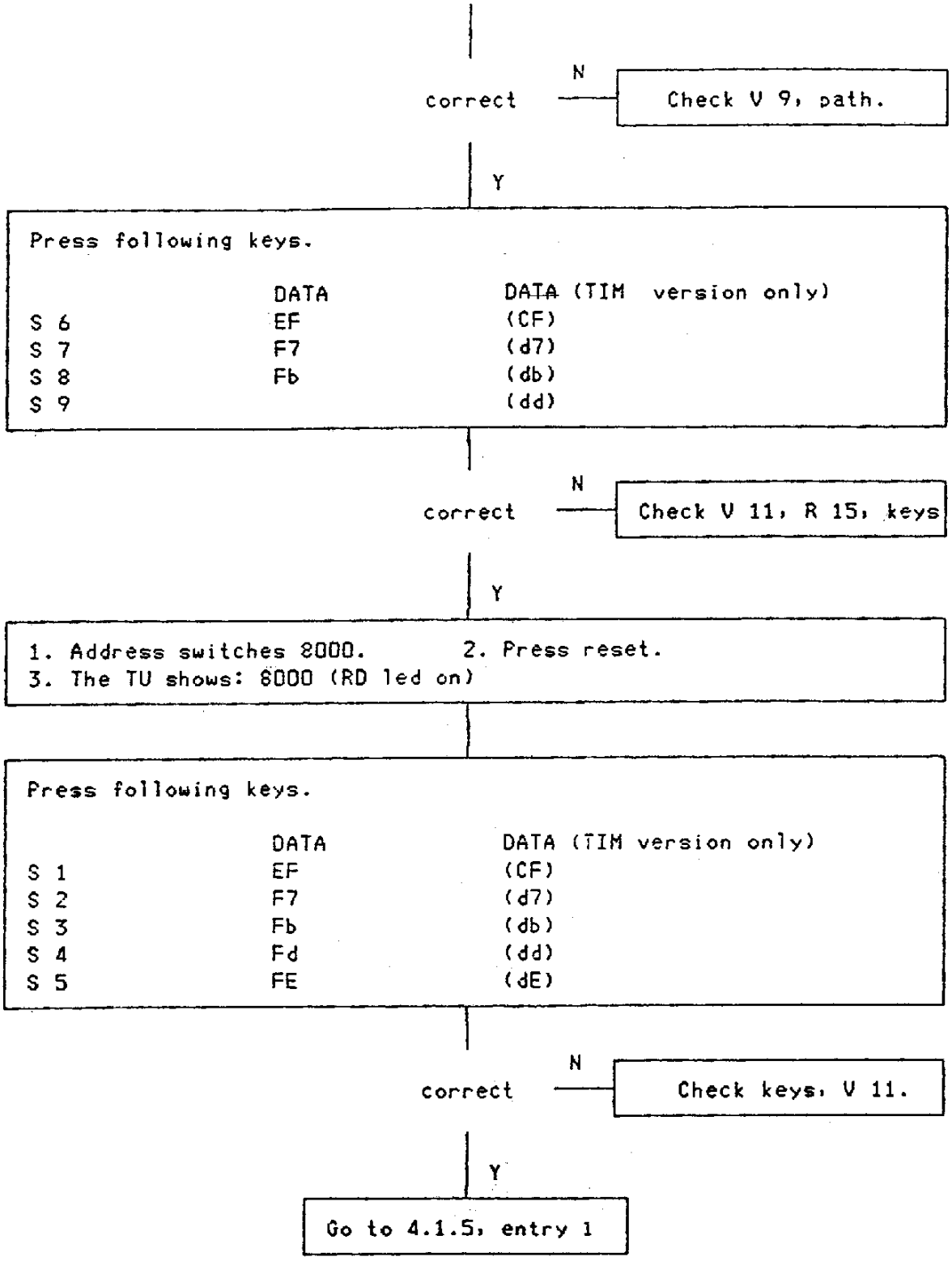


3.B FLOWCHART: Processor keyboard display PCB

(all measuring takes place on the processor keyboard display PCB)

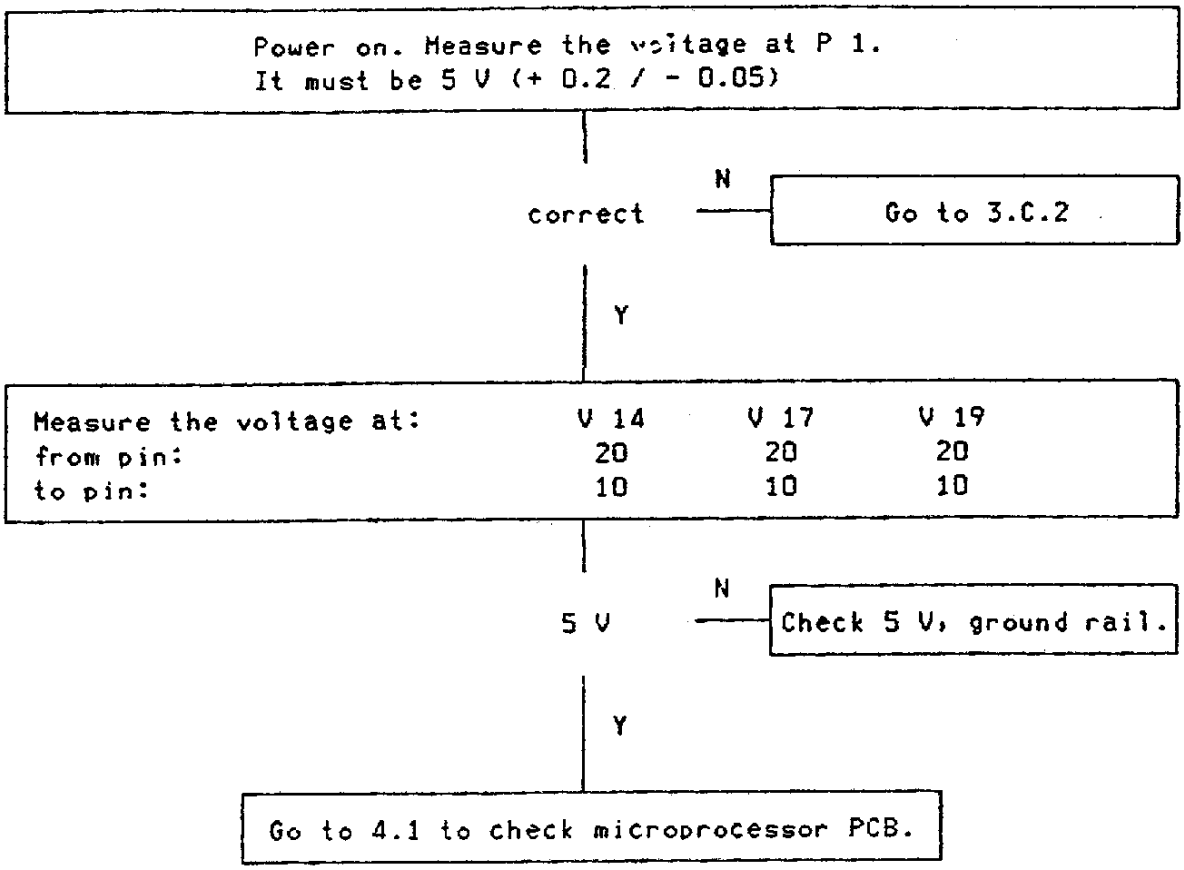



Measure the levels at V 9: pins 6 8 11
all H
N
Replace V 9.Check paths
Y
1. Set the address switches to 8003.
2. Press reset.
3. Measure the levels at V 9: 6 = L 8 = H 11 = H
correct
N
Check V 9.
jump with Elite 2000
Y
TIM and MOT variants only.
Press the following keys
DATA
TIM S 10 CF
MOT S 11 F7
S 12 Fb
S 13 Fd
correct
N
Check V 11, keys.
Y
1. Address switches 8005.
The TU shows: 8005 FF (dF *)
2. Press reset.
(*) ELITE 2000 TIM
Measure the levels at V 9: 6 = H 8 = L 11 = H

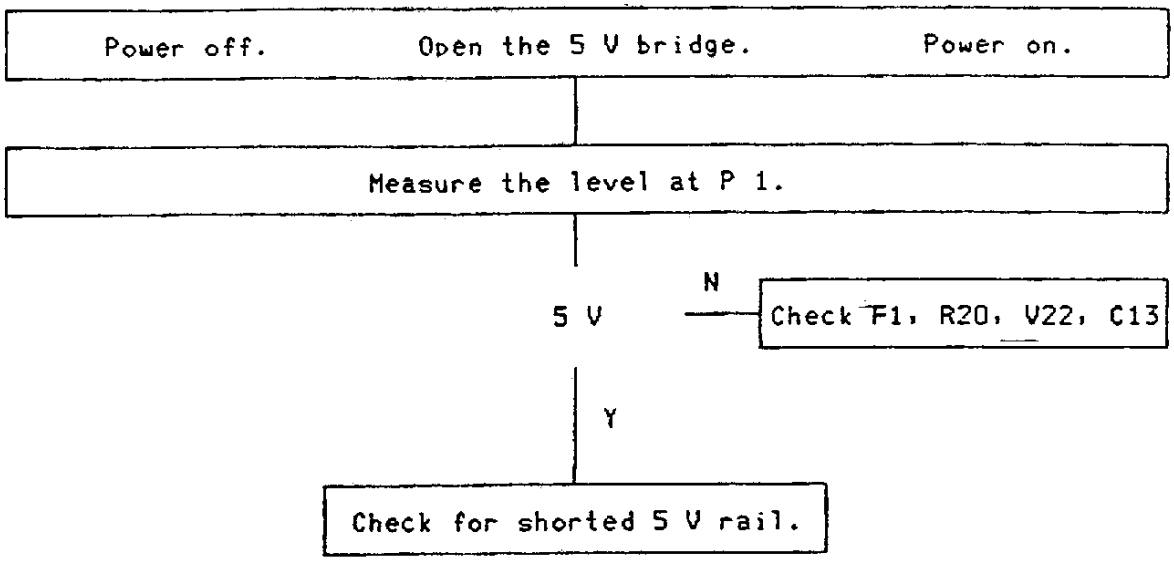

correct
N
Check V 9, path.
Y
Press following keys.
DATA
DATA (TIM version only)
S 6
EF
(CF)
S 7
F7
(d7)
S 8
Fb
(db)
S 9
(dd)
correct
N
Check V 11, R 15, keys
Y
1. Address switches 8000.
2. Press reset.
3. The TU shows: 8000 (RD led on)
Press following keys.
DATA
DATA (TIM version only)
S 1
EF
(CF)
S 2
F7
(d7)
S 3
Fb
(db)
S 4
Fd
(dd)
S 5
FE
(dE)
correct
N
Check keys, V 11.
Y
Go to 4.1.5, entry 1

3.C FLOWCHART: Power supply

All measuring refers to PCB power control.



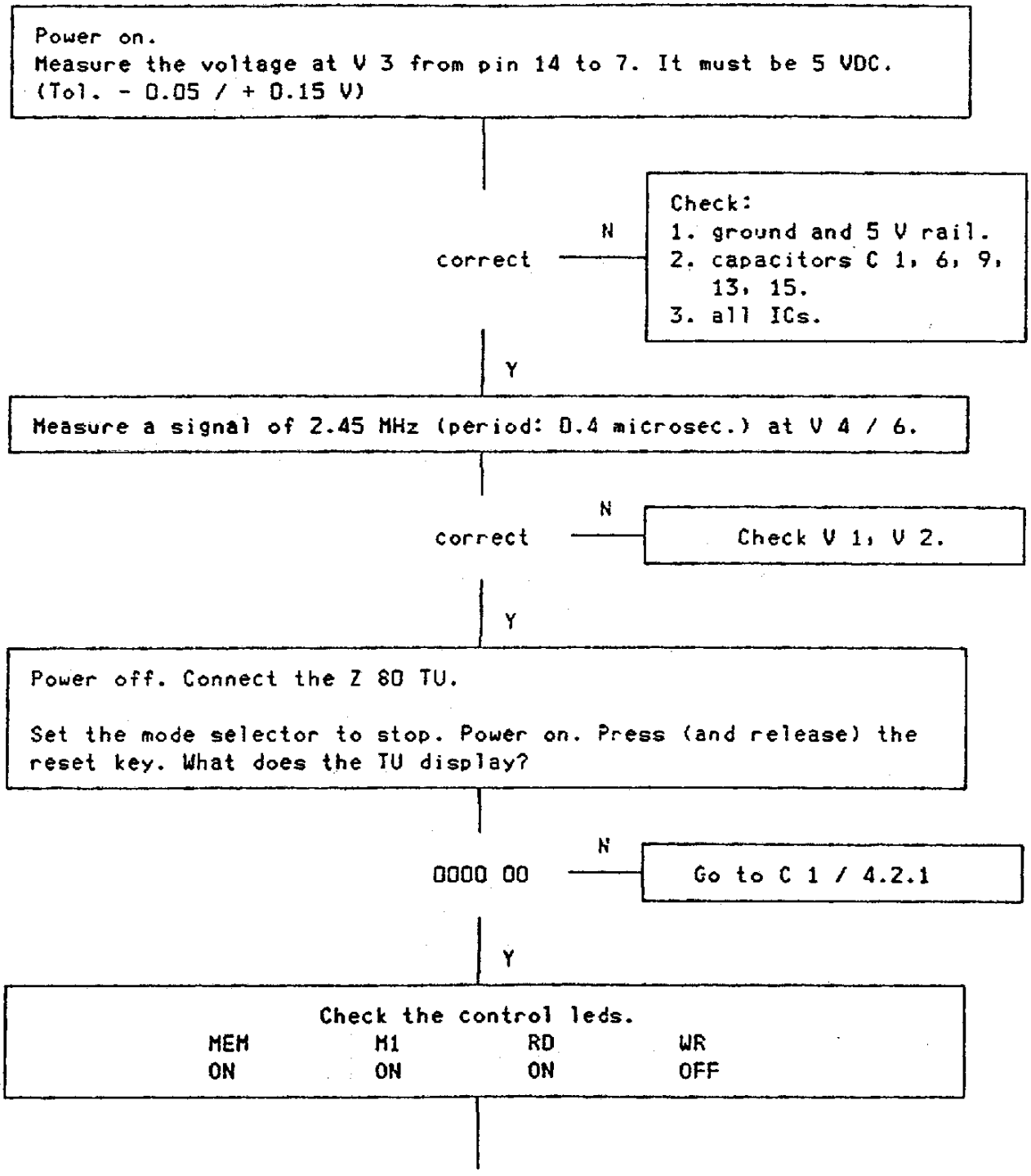
END

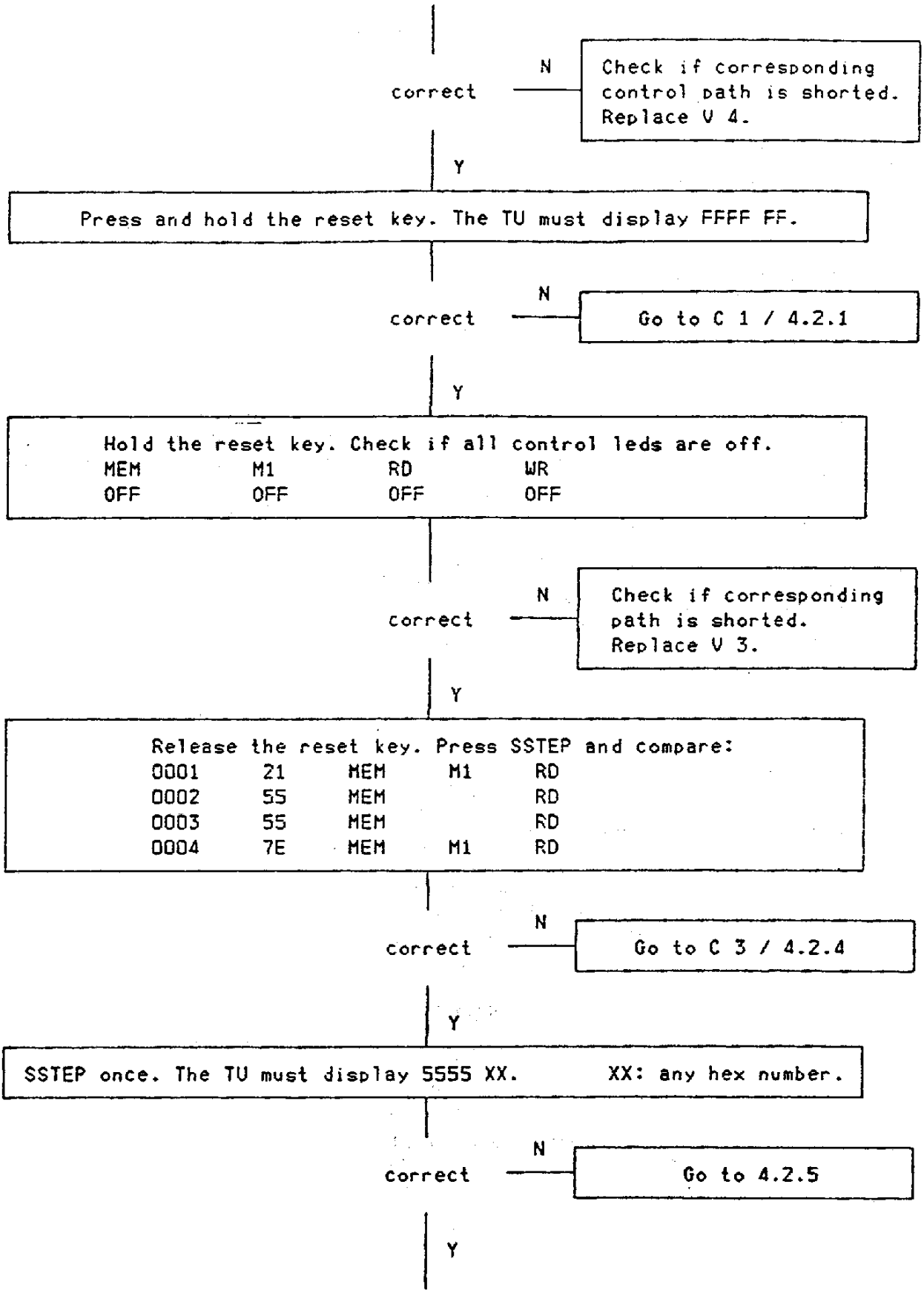

Power off.
Open the 5 V bridge.
Power on.
Measure the level at P 1.
5 V
N
Check F1, R20, V22, C13
Y
Check for shorted 5 V rail.

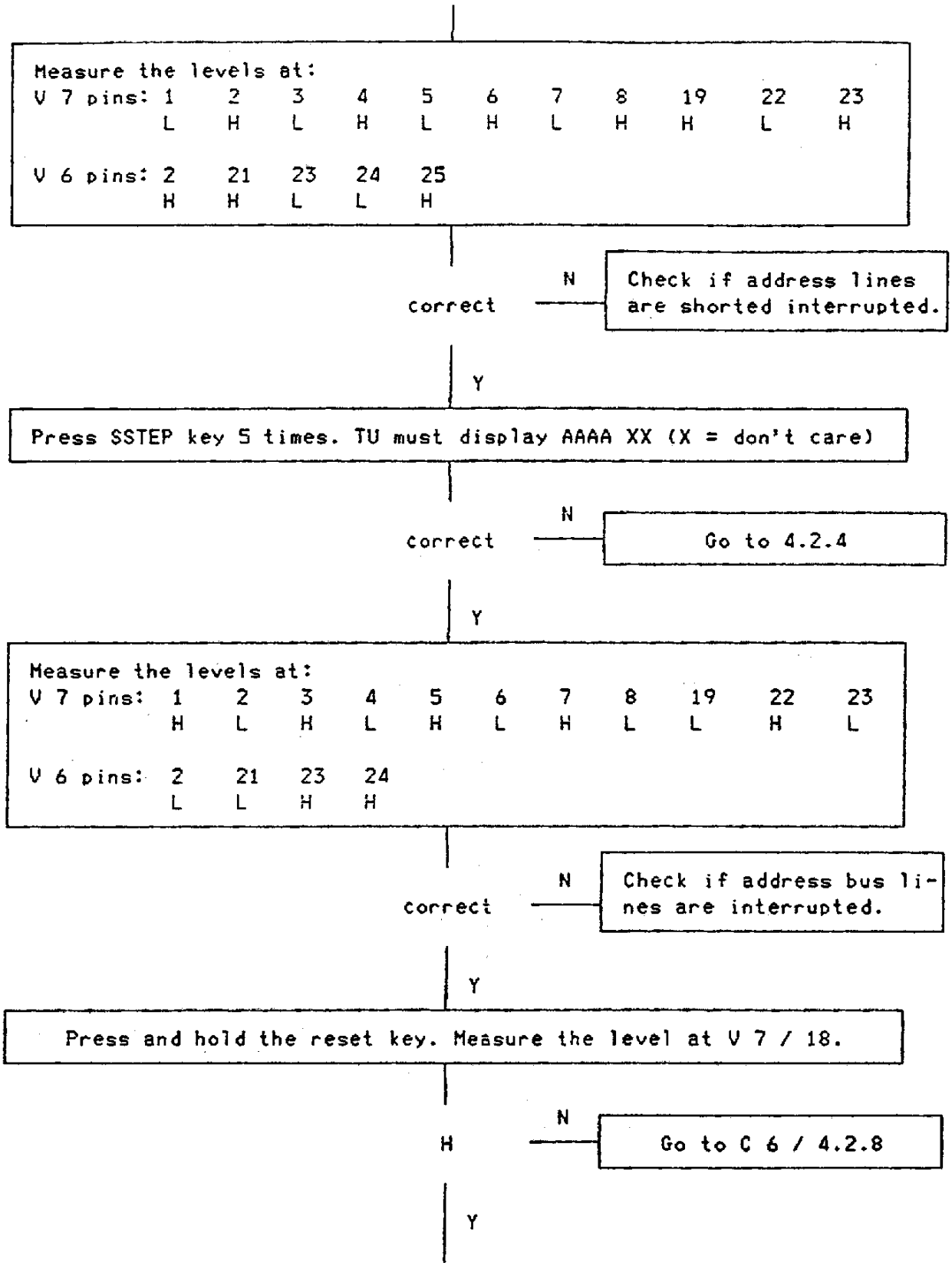
END

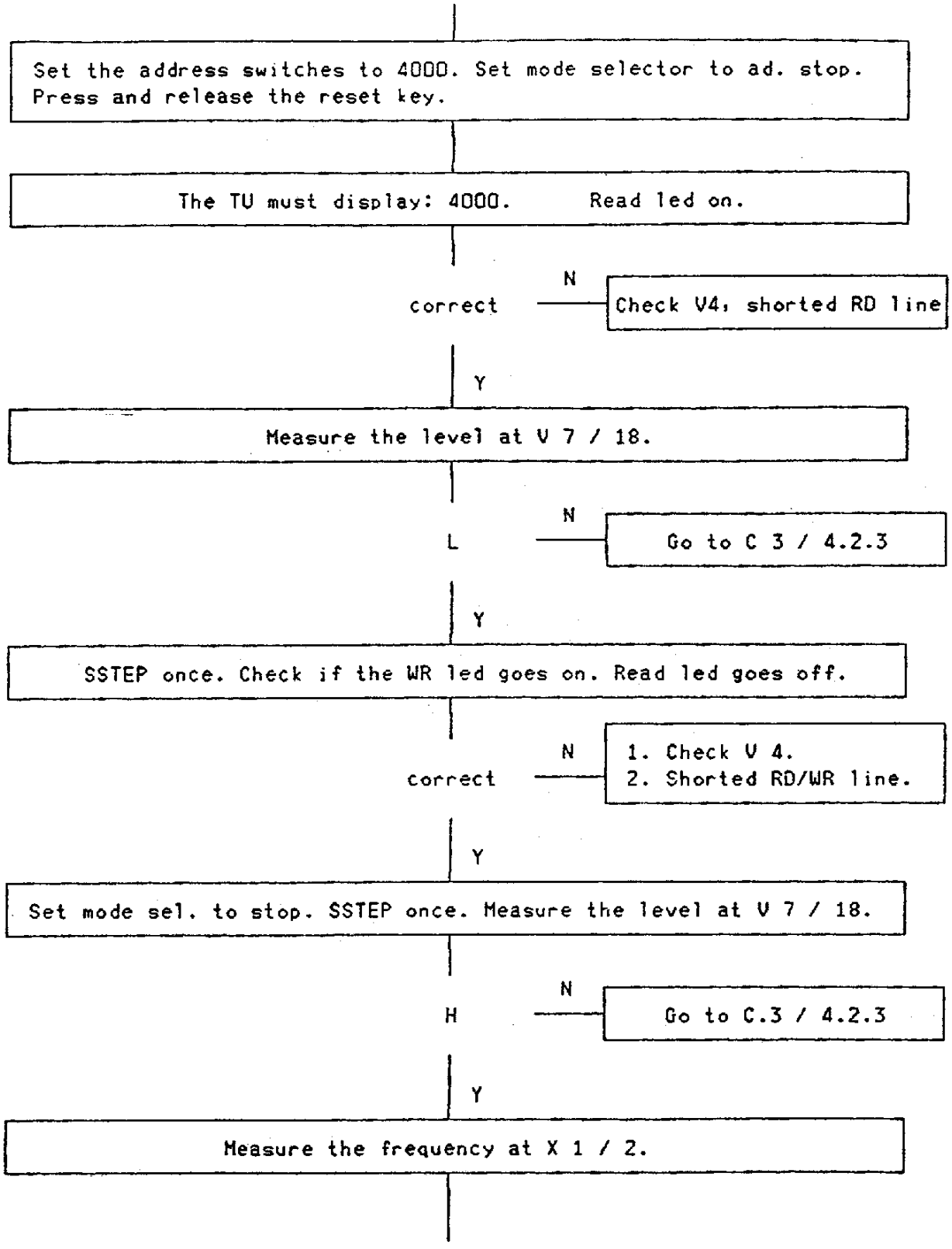
4.1 PROCESSOR PCB

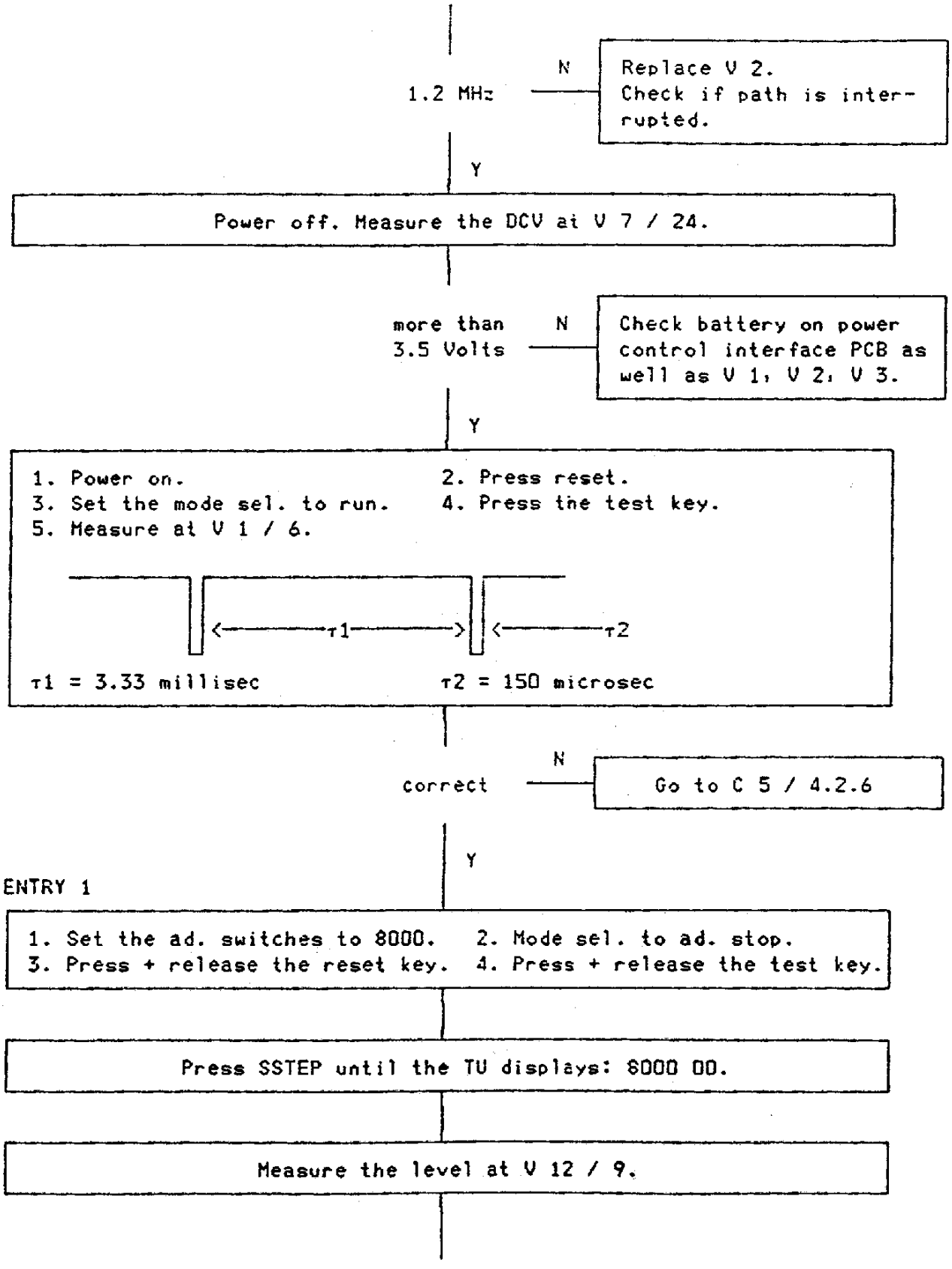
Note:
All ICs mentioned throughout this section are located on the microprocessor board: MA60345

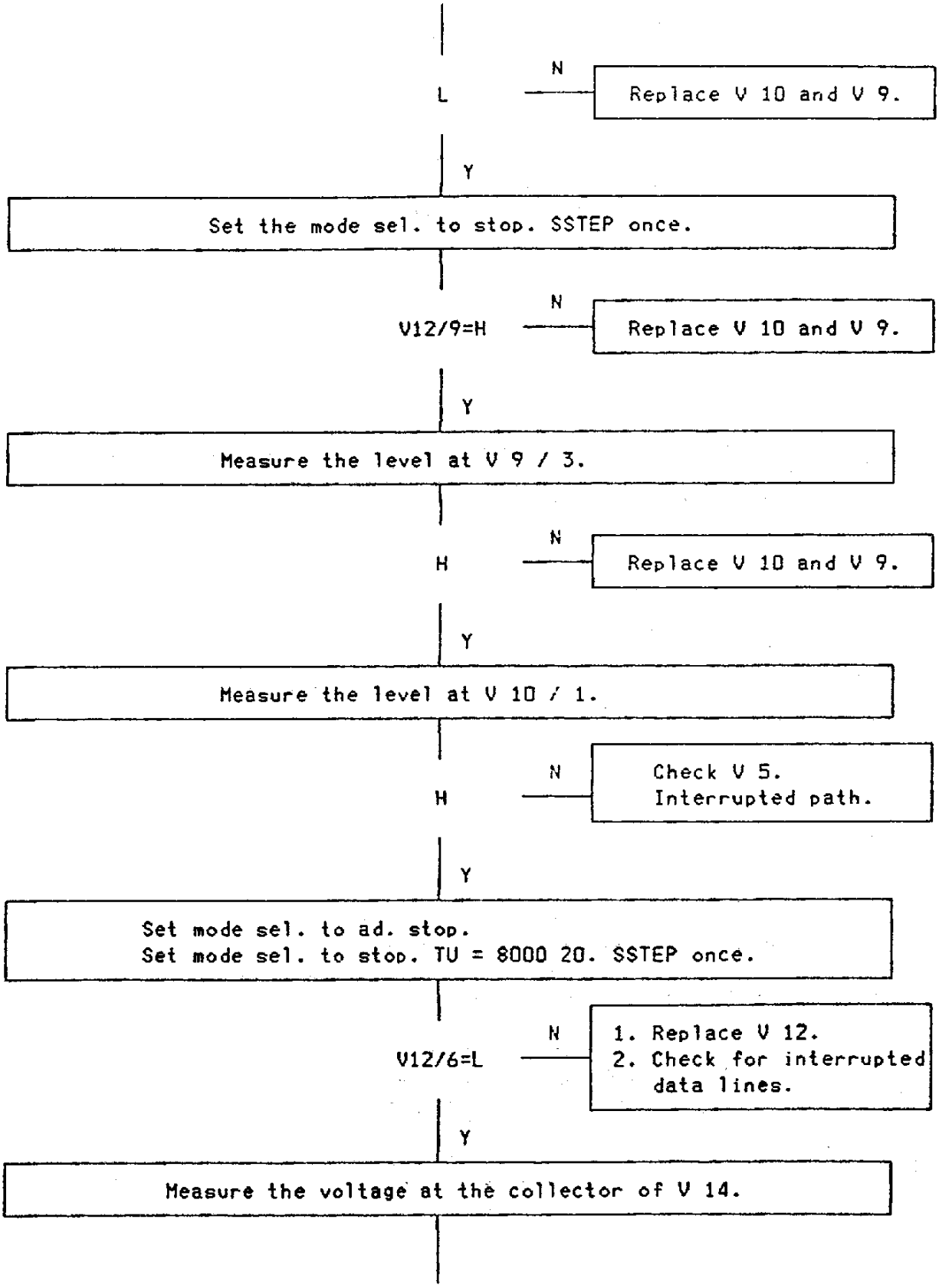


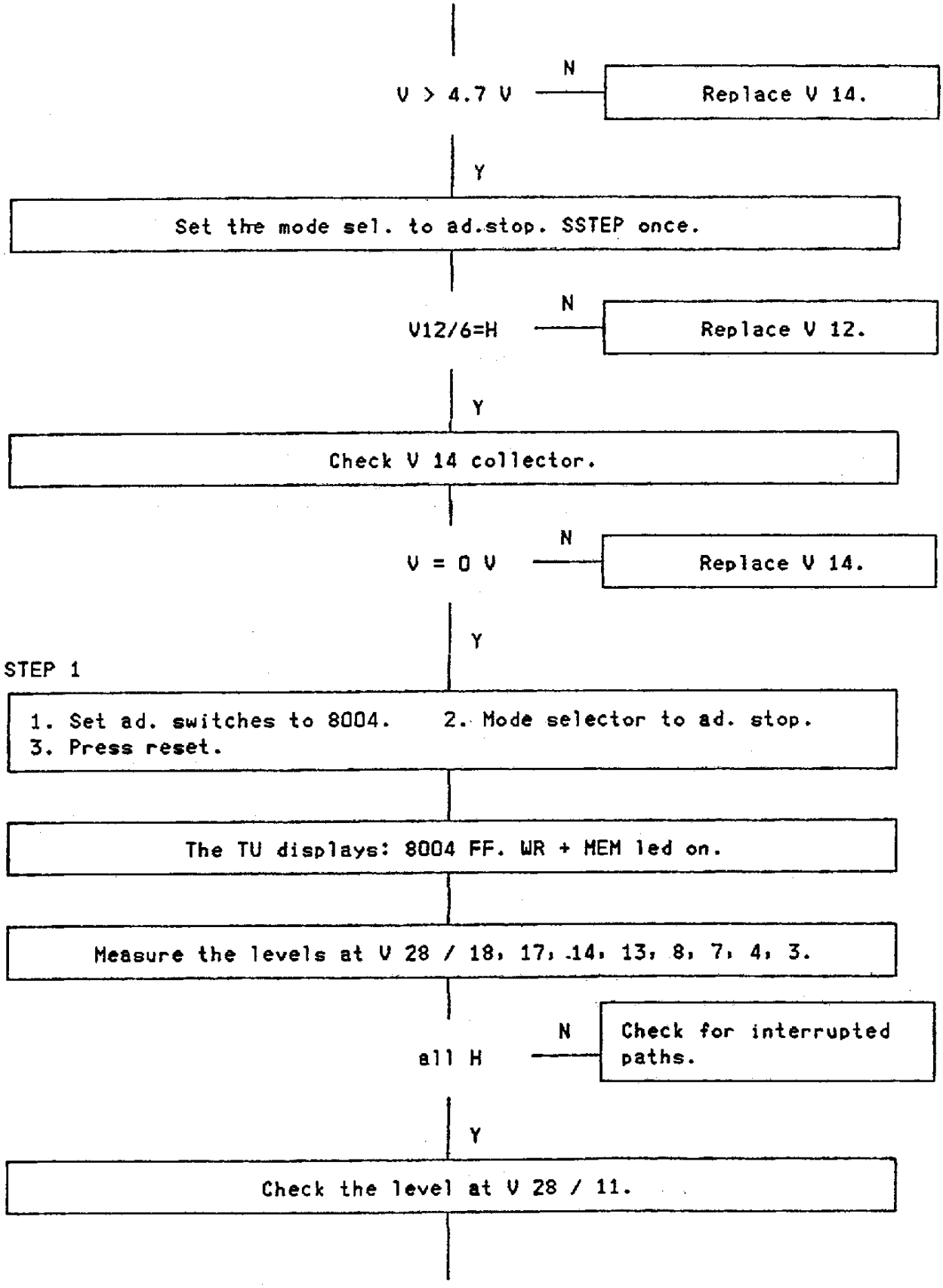

correct
N
Check if corresponding control path is shorted. Replace V 4.
Y
Press and hold the reset key. The TU must display FFFF FF.
correct
N
Go to C 1 / 4.2.1
Y
Hold the reset key. Check if all control leds are off.
MEM M1 RD WR
OFF OFF OFF OFF
correct
N
Check if corresponding path is shorted. Replace V 3.
Y
Release the reset key. Press SSTEP and compare:
0001 21 MEM M1 RD
0002 55 MEM RD
0003 55 MEM RD
0004 7E MEM M1 RD
correct
N
Go to C 3 / 4.2.4
Y
SSTEP once. The TU must display 5555 XX. XX: any hex number.
correct
N
Go to 4.2.5
Y

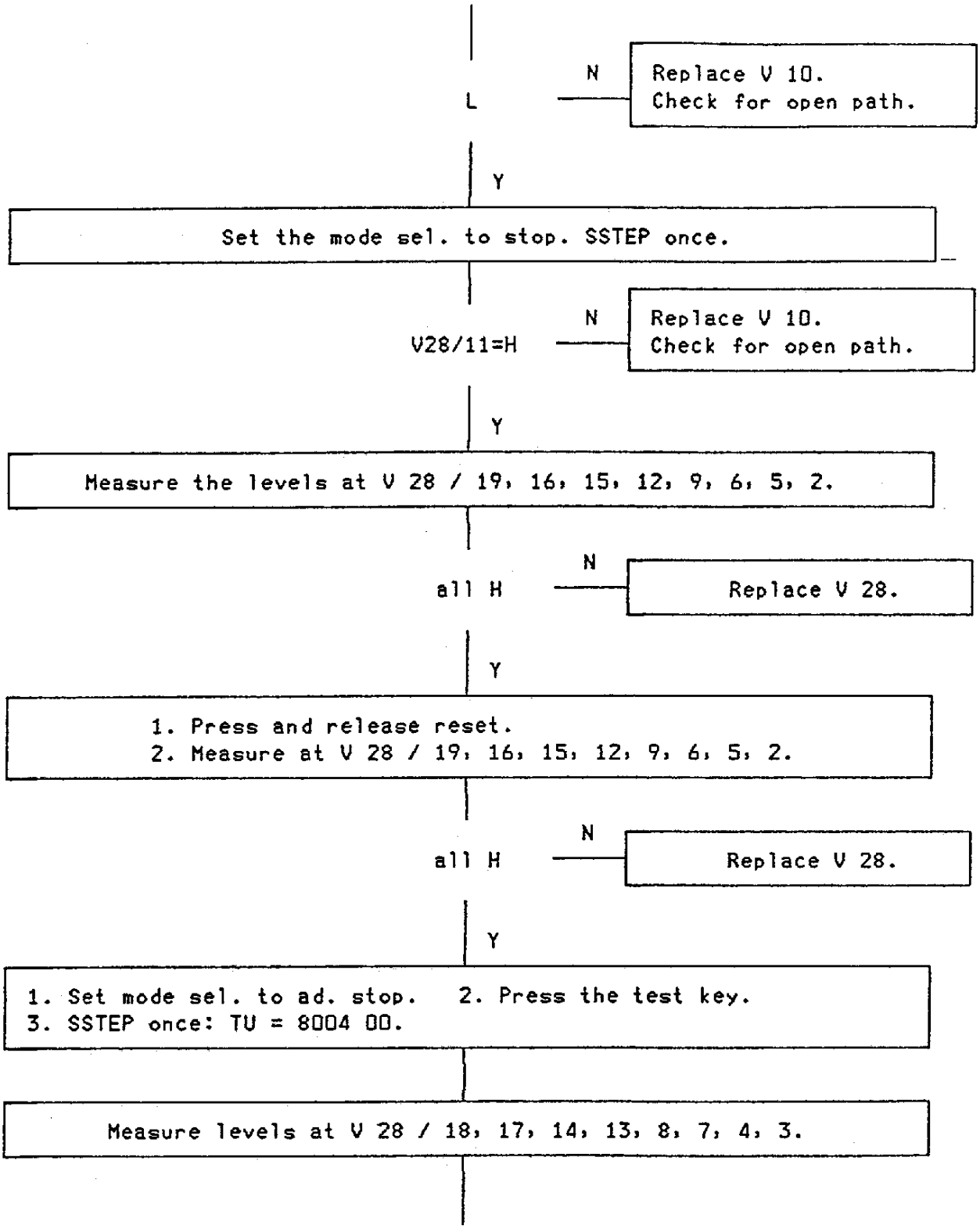

Measure the levels at:
V 7 pins: 1 2 3 4 5 6 7 8 19 22 23
L H L H L H L H H L H
V 6 pins: 2 21 23 24 25
H H L L H
correct
N
Check if address lines are shorted interrupted.
Y
Press SSTEP key 5 times. TU must display AAAA XX (X = don't care)
correct
N
Go to 4.2.4
Y
Measure the levels at:
V 7 pins: 1 2 3 4 5 6 7 8 19 22 23
H L H L H L H L L H L
V 6 pins: 2 21 23 24
L L H H
correct
N
Check if address bus lines are interrupted.
Y
Press and hold the reset key. Measure the level at V 7 / 18.
H
N
Go to C 6 / 4.2.8
Y

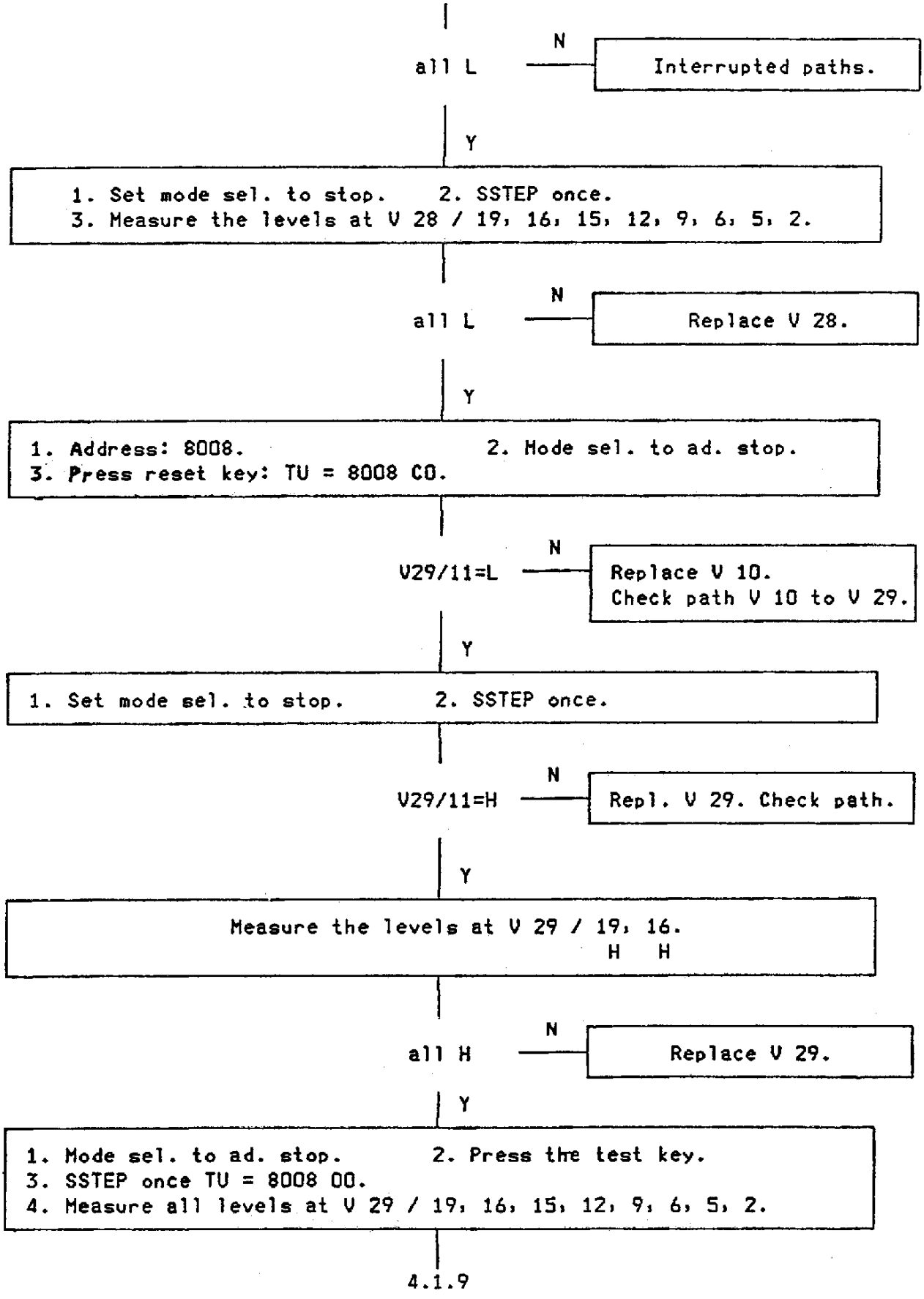

Set the address switches to 4000. Set mode selector to ad. stop.
Press and release the reset key.
The TU must display: 4000. Read led on.
correct
N
Check V4, shorted RD line
Y
Measure the level at V 7 / 18.
L
N
Go to C 3 / 4.2.3
Y
SSTEP once. Check if the WR led goes on. Read led goes off.
correct
N
1. Check V 4.
2. Shorted RD/WR line.
Y
Set mode sel. to stop. SSTEP once. Measure the level at V 7 / 18.
H
N
Go to C.3 / 4.2.3
Y
Measure the frequency at X 1 / 2.

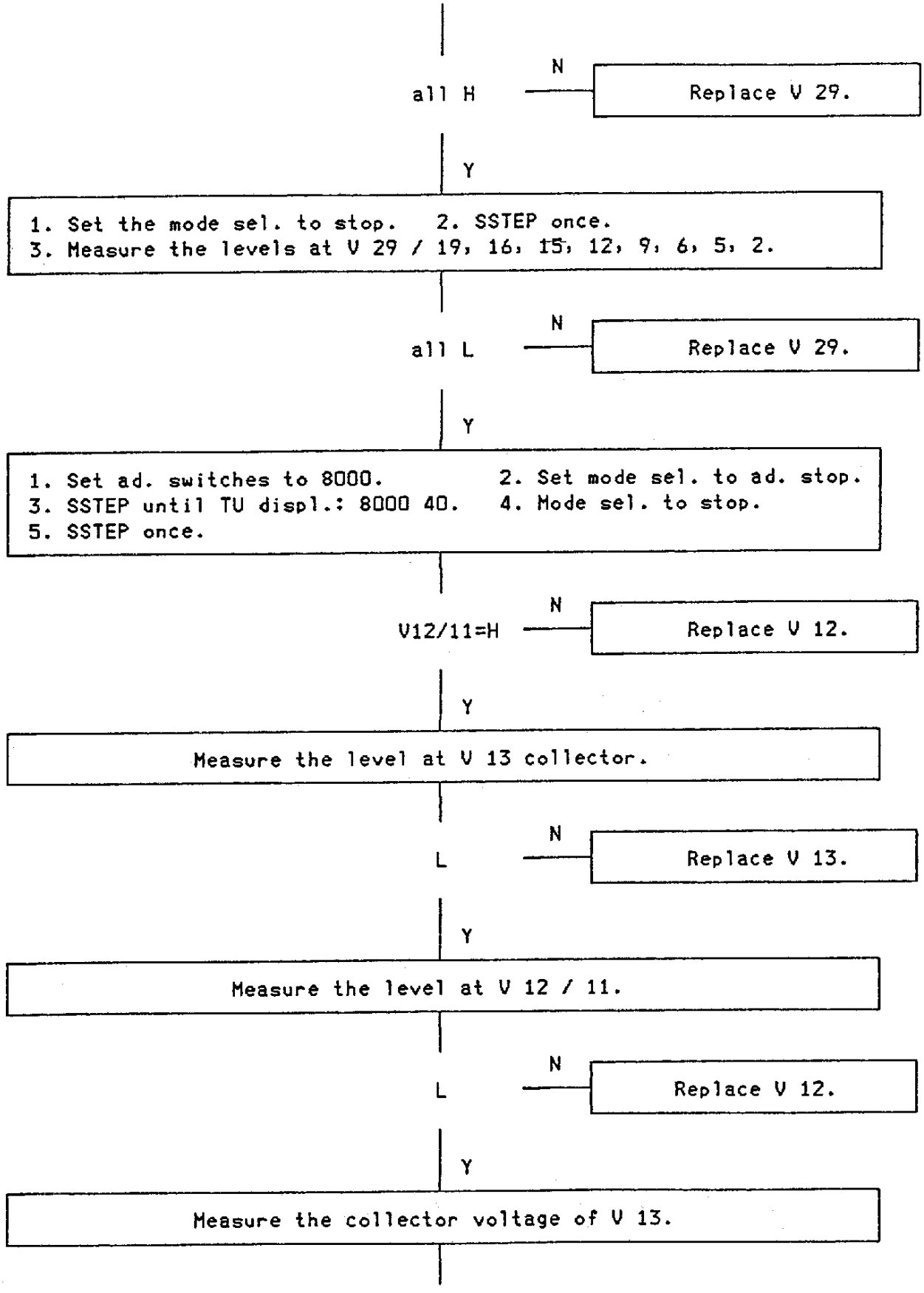

1.2 MHz
N
Replace V 2.
Check if path is interrupted.
Y
Power off. Measure the DCV at V 7 / 24.
more than 3.5 Volts
N
Check battery on power control interface PCB as well as V 1, V 2, V 3.
Y
1. Power on.
2. Press reset.
3. Set the mode sel. to run.
4. Press the test key.
5. Measure at V 1 / 6.
τ1
τ2
τ1 = 3.33 millisec
τ2 = 150 microsec
correct
N
Go to C 5 / 4.2.6
Y
ENTRY 1
1. Set the ad. switches to 8000.
2. Mode sel. to ad. stop.
3. Press + release the reset key.
4. Press + release the test key.
Press SSTEP until the TU displays: 8000 00.
Measure the level at V 12 / 9.

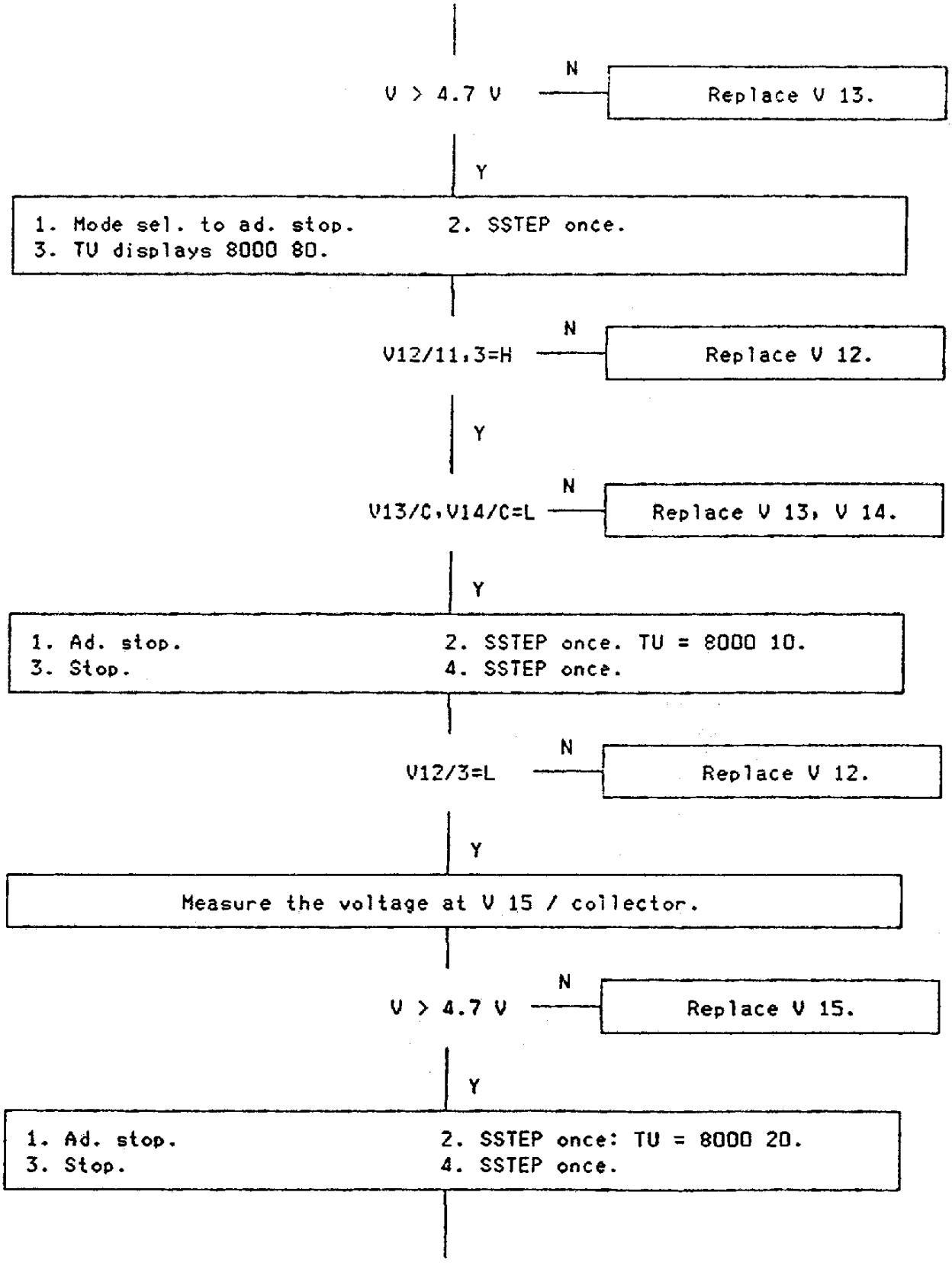

L
N
Replace V 10 and V 9.
Y
Set the mode sel. to stop. SSTEP once.
V12/9=H
N
Replace V 10 and V 9.
Y
Measure the level at V 9 / 3.
H
N
Replace V 10 and V 9.
Y
Measure the level at V 10 / 1.
H
N
Check V 5.
Interrupted path.
Y
Set mode sel. to ad. stop.
Set mode sel. to stop. TU = 8000 20. SSTEP once.
V12/6=L
N
1. Replace V 12.
2. Check for interrupted data lines.
Y
Measure the voltage at the collector of V 14.

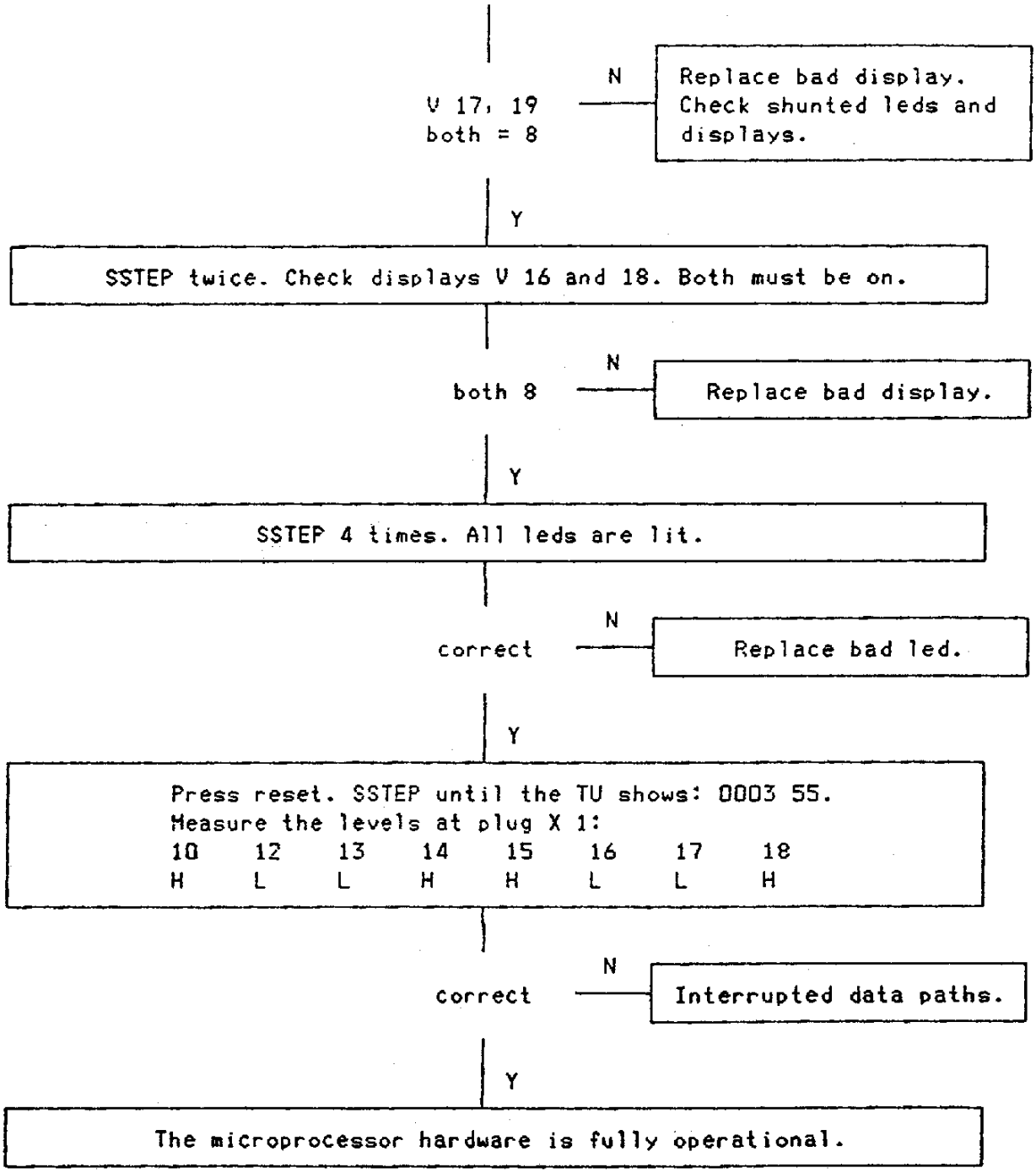

V > 4.7 V
N
Replace V 14.
Y
Set the mode sel. to ad.stop. SSTEP once.
V12/6=H
N
Replace V 12.
Y
Check V 14 collector.
V = 0 V
N
Replace V 14.
Y
STEP 1
1. Set ad. switches to 8004. 2. Mode selector to ad. stop.
3. Press reset.
The TU displays: 8004 FF. WR + MEM led on.
Measure the levels at V 28 / 18, 17, 14, 13, 8, 7, 4, 3.
all H
N
Check for interrupted paths.
Y
Check the level at V 28 / 11.

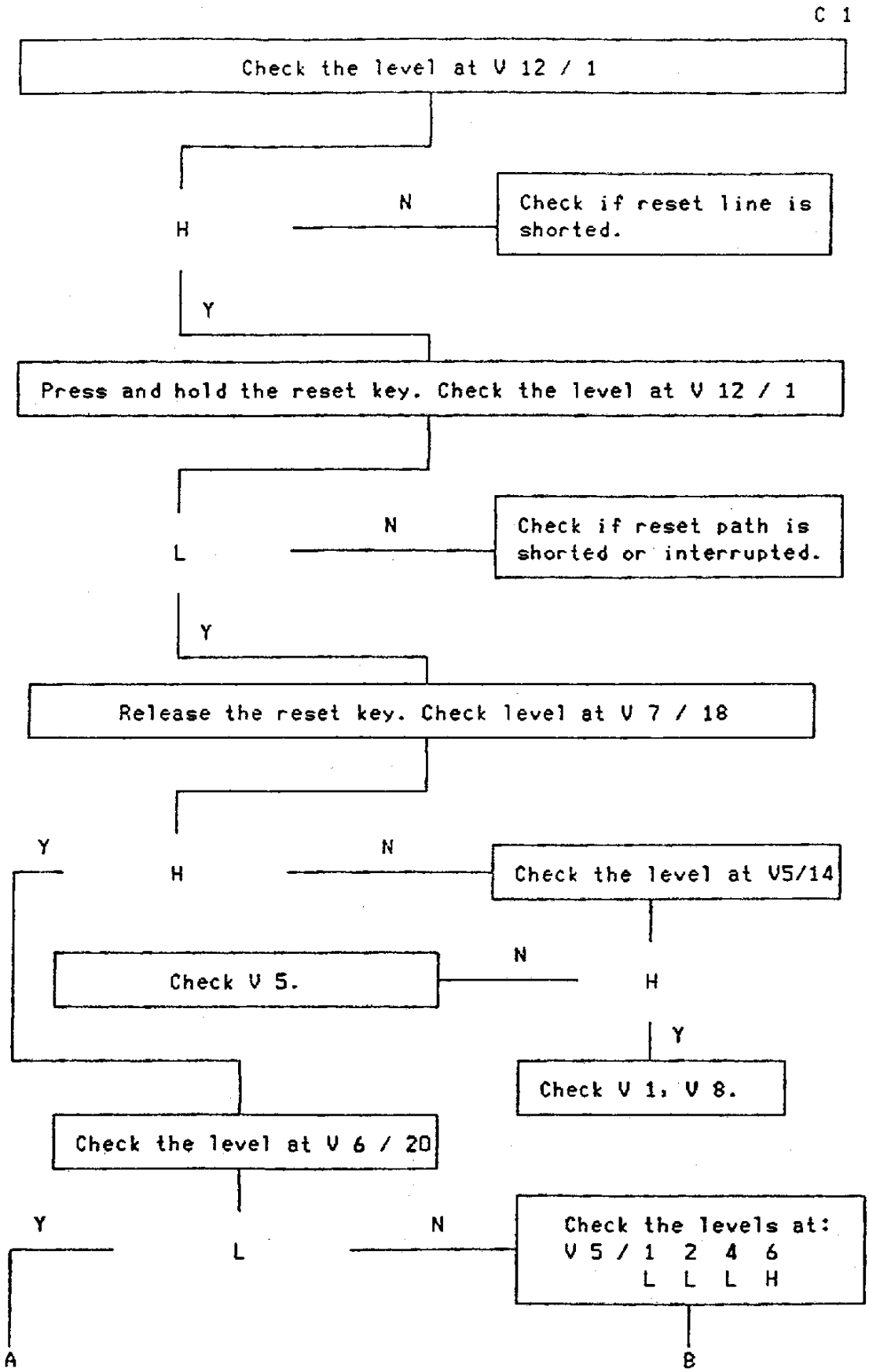

L
N
Replace V 10.
Check for open path.
Y
Set the mode sel. to stop. SSTEP once.
V28/11=H
N
Replace V 10.
Check for open path.
Y
Measure the levels at V 28 / 19, 16, 15, 12, 9, 6, 5, 2.
all H
N
Replace V 28.
Y
1. Press and release reset.
2. Measure at V 28 / 19, 16, 15, 12, 9, 6, 5, 2.
all H
N
Replace V 28.
Y
1. Set mode sel. to ad. stop. 2. Press the test key.
3. SSTEP once: TU = 8004 00.
Measure levels at V 28 / 18, 17, 14, 13, 8, 7, 4, 3.

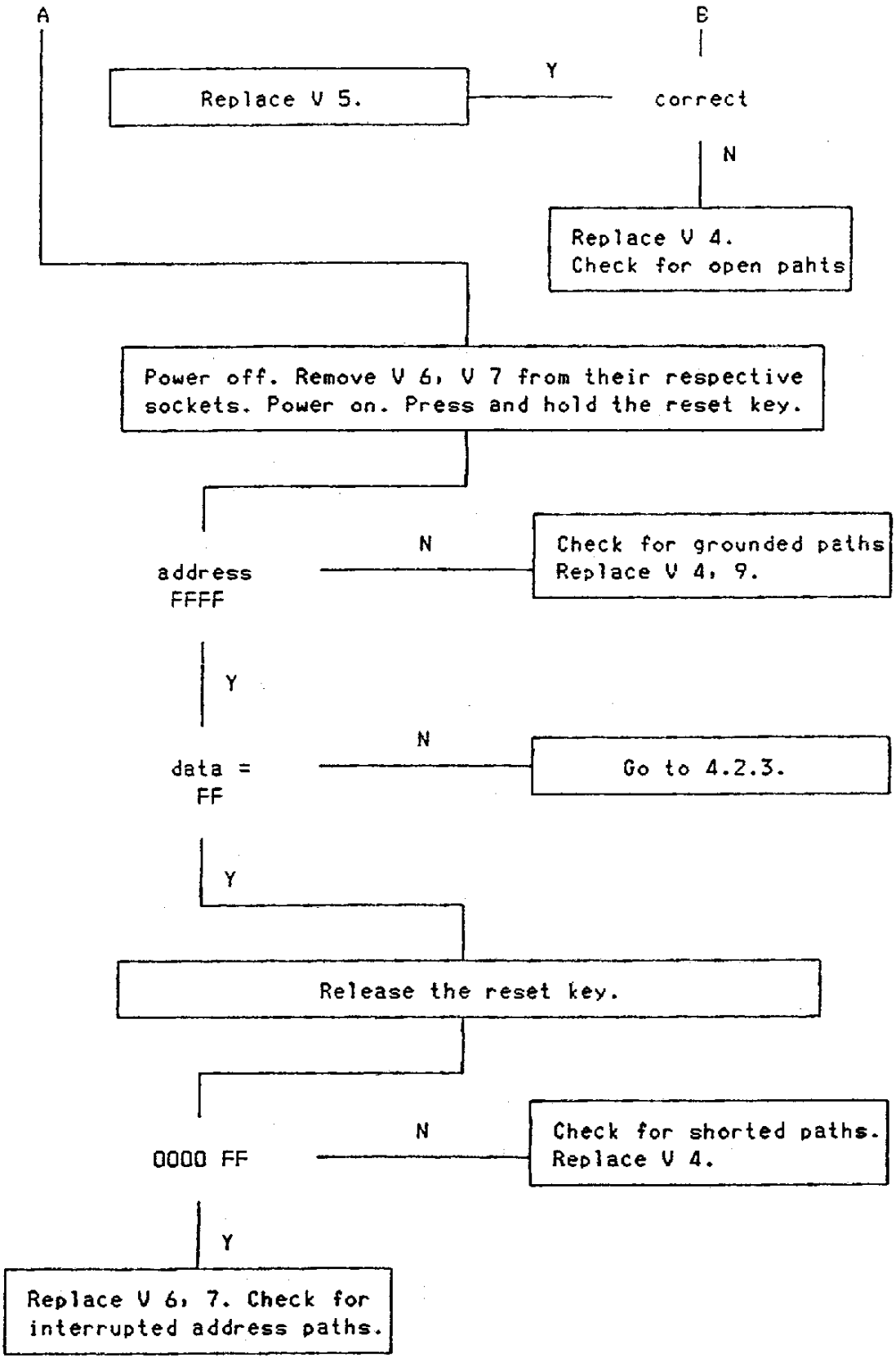

all L
N
Interrupted paths.
Y
1. Set mode sel. to stop. 2. SSTEP once.
3. Measure the levels at V 28 / 19, 16, 15, 12, 9, 6, 5, 2.
all L
N
Replace V 28.
Y
1. Address: 8008. 2. Mode sel. to ad. stop.
3. Press reset key: TU = 8008 CO.
V29/11=L
N
Replace V 10.
Check path V 10 to V 29.
Y
1. Set mode sel. to stop. 2. SSTEP once.
V29/11=H
N
Repl. V 29. Check path.
Y
Measure the levels at V 29 / 19, 16.
H H
all H
N
Replace V 29.
Y
1. Mode sel. to ad. stop. 2. Press the test key.
3. SSTEP once TU = 8008 00.
4. Measure all levels at V 29 / 19, 16, 15, 12, 9, 6, 5, 2.
4.1.9

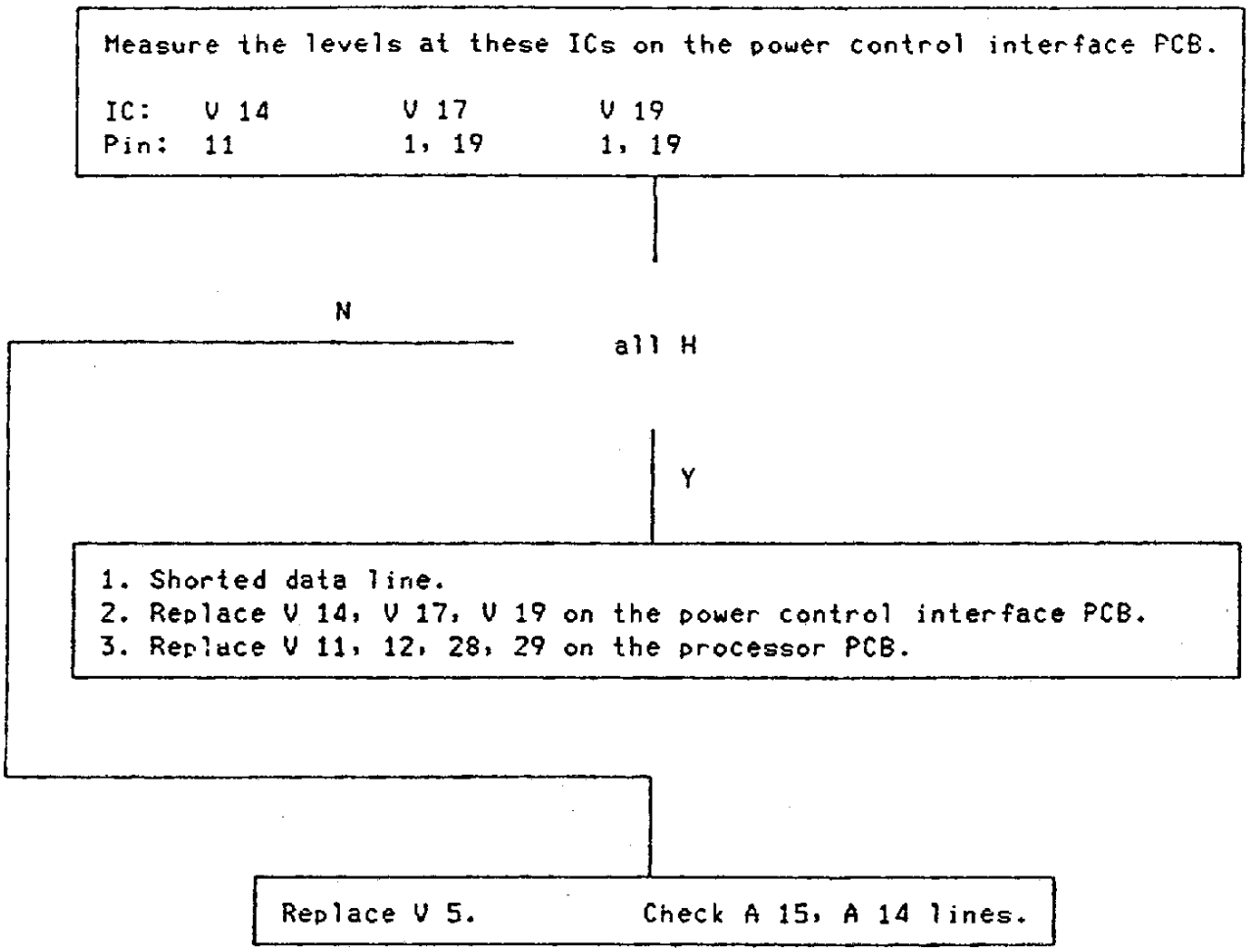

all H
N
Replace V 29.
Y
1. Set the mode sel. to stop. 2. SSTEP once.
3. Measure the levels at V 29 / 19, 16, 15, 12, 9, 6, 5, 2.
all L
N
Replace V 29.
Y
1. Set ad. switches to 8000. 2. Set mode sel. to ad. stop.
3. SSTEP until TU displ.: 8000 40. 4. Mode sel. to stop.
5. SSTEP once.
V12/11=H
N
Replace V 12.
Y
Measure the level at V 13 collector.
L
N
Replace V 13.
Y
Measure the level at V 12 / 11.
L
N
Replace V 12.
Y
Measure the collector voltage of V 13.


V > 4.7 V
N
Replace V 13.
Y
1. Mode sel. to ad. stop.
2. SSTEP once.
3. TU displays 8000 80.
V12/11,3=H
N
Replace V 12.
Y
V13/C,V14/C=L
N
Replace V 13, V 14.
Y
1. Ad. stop.
2. SSTEP once. TU = 8000 10.
3. Stop.
4. SSTEP once.
V12/3=L
N
Replace V 12.
Y
Measure the voltage at V 15 / collector.
V > 4.7 V
N
Replace V 15.
Y
1. Ad. stop.
2. SSTEP once: TU = 8000 20.
3. Stop.
4. SSTEP once.

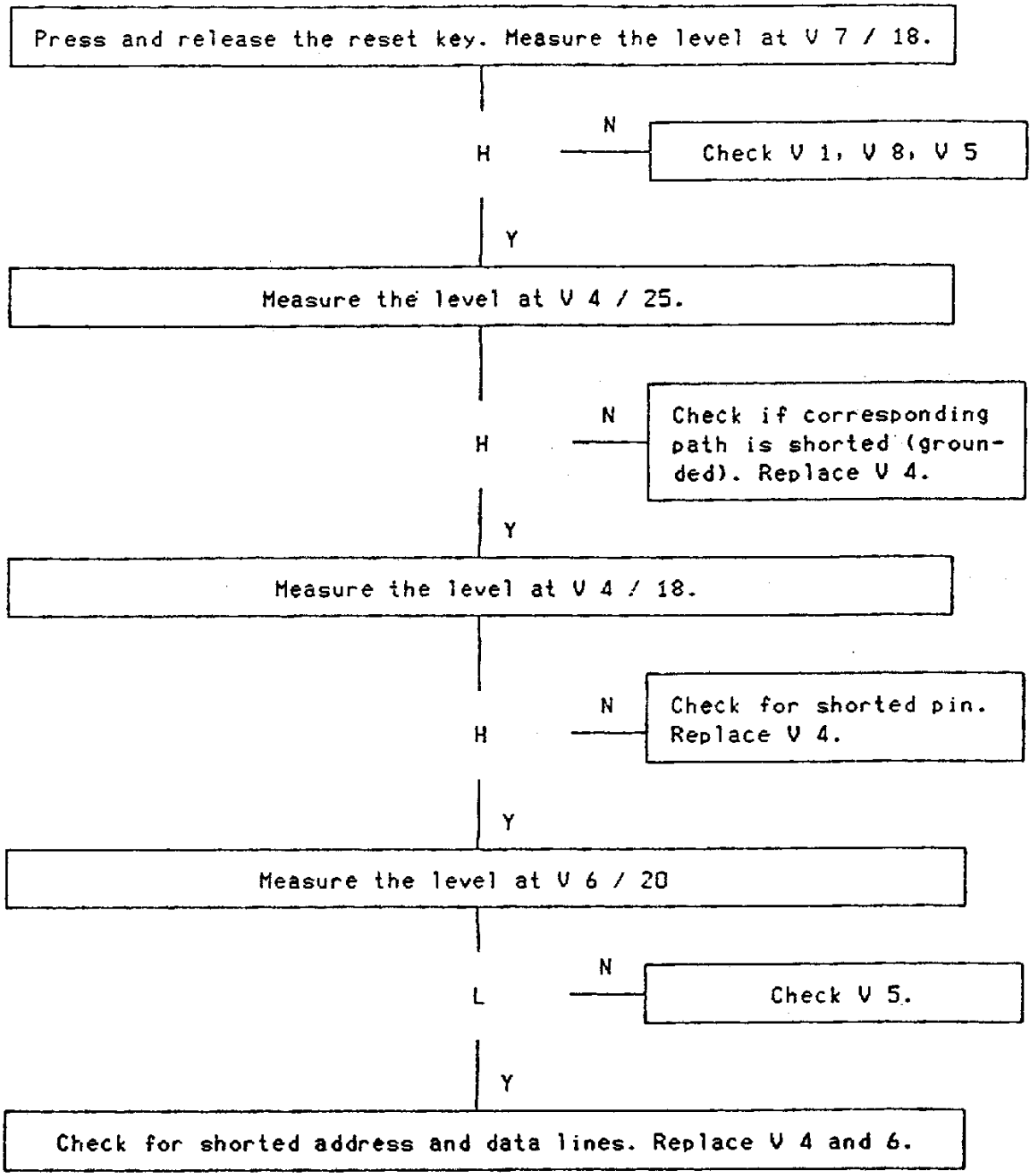

V 17, 19
both = 8
N
Replace bad display.
Check shunted leds and displays.
Y
SSTEP twice. Check displays V 16 and 18. Both must be on.
both 8
N
Replace bad display.
Y
SSTEP 4 times. All leds are lit.
correct
N
Replace bad led.
Y
Press reset. SSTEP until the TU shows: 0003 55.
Measure the levels at plug X 1:
10 12 13 14 15 16 17 18
H L L H H L L H
correct
N
Interrupted data paths.
Y
The microprocessor hardware is fully operational.


C 1
Check the level at V 12 / 1
H
N
Check if reset line is shorted.
Y
Press and hold the reset key. Check the level at V 12 / 1
L
N
Check if reset path is shorted or interrupted.
Y
Release the reset key. Check level at V 7 / 18
Y
H
N
Check the level at V5/14
Check V 5.
N
H
Y
Check V 1, V 8.
Check the level at V 6 / 20
Y
L
N
Check the levels at:
V 5 / 1 2 4 6
L L L H
A
B


A
B
Y
Replace V 5.
correct
N
Replace V 4.
Check for open pahts
Power off. Remove V 6, V 7 from their respective sockets. Power on. Press and hold the reset key.
address FFFF
N
Check for grounded paths
Replace V 4, 9.
Y
data = FF
N
Go to 4.2.3.
Y
Release the reset key.
0000 FF
N
Check for shorted paths.
Replace V 4.
Y
Replace V 6, 7. Check for interrupted address paths.


Measure the levels at these ICs on the power control interface PCB.
IC: V 14 V 17 V 19
Pin: 11 1, 19 1, 19
N
all H
Y
1. Shorted data line.
2. Replace V 14, V 17, V 19 on the power control interface PCB.
3. Replace V 11, 12, 28, 29 on the processor PCB.
Replace V 5.
Check A 15, A 14 lines.

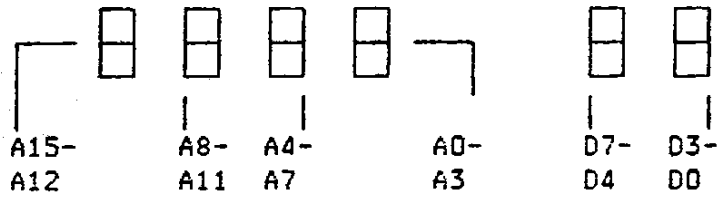
C 3


Press and release the reset key. Measure the level at V 7 / 18.
H
N
Check V 1, V 8, V 5
Y
Measure the level at V 4 / 25.
H
N
Check if corresponding path is shorted (grounded). Replace V 4.
Y
Measure the level at V 4 / 18.
H
N
Check for shorted pin. Replace V 4.
Y
Measure the level at V 6 / 20
L
N
Check V 5.
Y
Check for shorted address and data lines. Replace V 4 and 6.

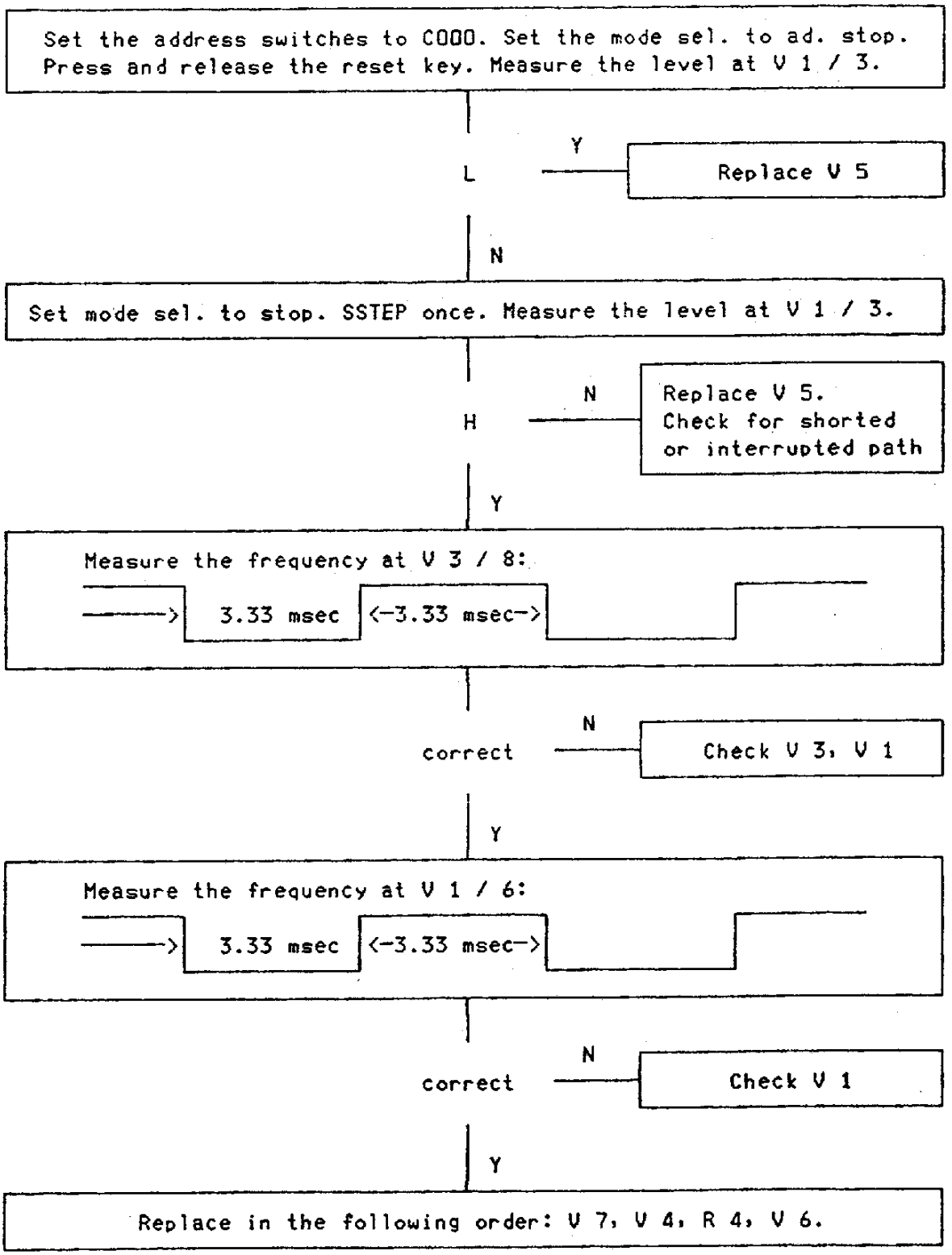
STEP 1 C 4

Shorted address / data lines.

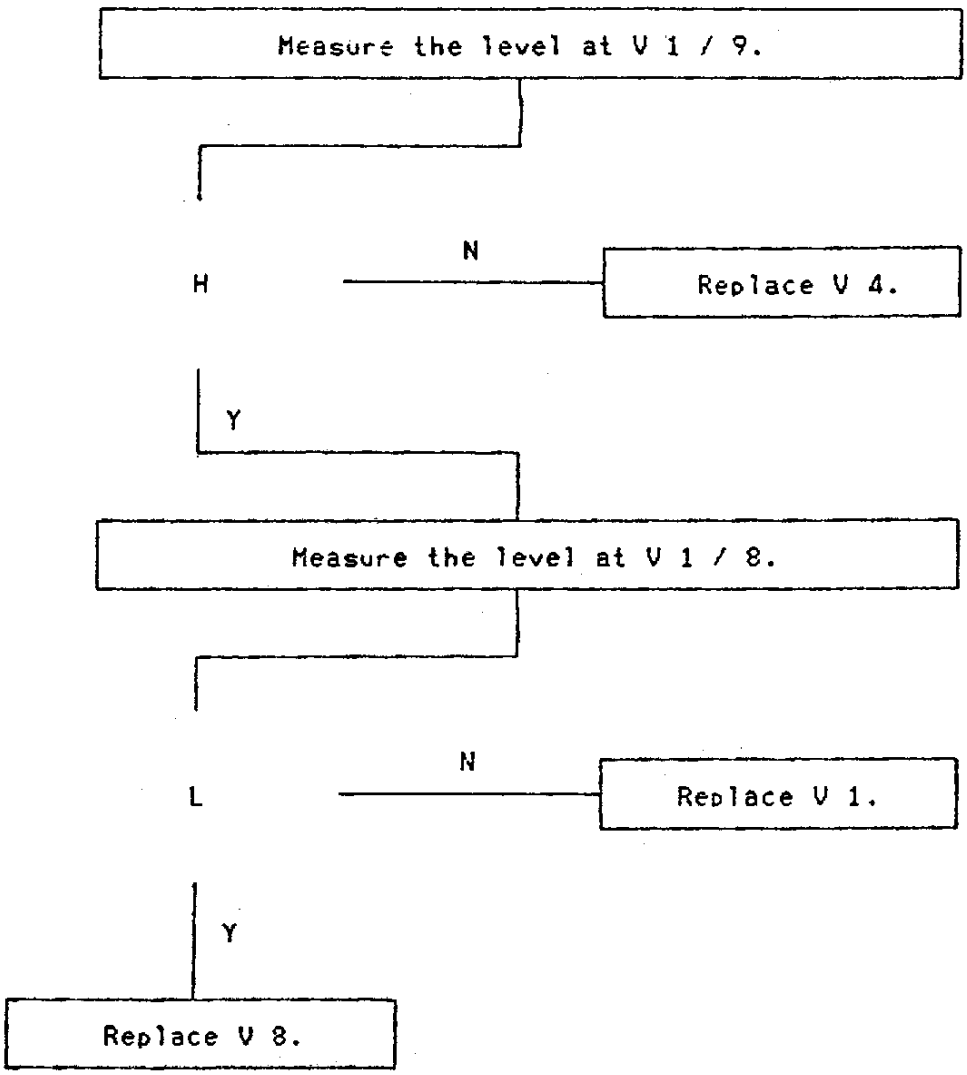
Each digit in the TU displays the state of four address and data lines respectively. As the Z 80 has 16 address and 8 data lines, the TU needs 4 digits to read the address bus and 2 digits to read the data bus. Each half-byte (4 bits) is represented in an hexadecimal number. Consequently the first digit on the TU, starting left, shows the logic states of address lines A 15 - A 12, the second one shows them from A 8 to A 11 and so on.



C 5


Set the address switches to C000. Set the mode sel. to ad. stop.
Press and release the reset key. Measure the level at V 1 / 3.
L
Y
Replace V 5
N
Set mode sel. to stop. SSTEP once. Measure the level at V 1 / 3.
H
N
Replace V 5.
Check for shorted
or interrupted path
Y
Measure the frequency at V 3 / 8:
3.33 msec
<-3.33 msec->
correct
N
Check V 3, V 1
Y
Measure the frequency at V 1 / 6:
3.33 msec
<-3.33 msec->
correct
N
Check V 1
Y
Replace in the following order: V 7, V 4, R 4, V 6.

C 6


Measure the level at V 1 / 9.
H
N
Replace V 4.
Y
Measure the level at V 1 / 8.
L
N
Replace V 1.
Y
Replace V 8.

5.5 INTERFACE PCB

The processor PCB must be operational. All measurings refers to the interface PCB.

Power off. Remove lens motor plug X 6 from the control desk.
Move head to midway (50 cm)

Measure the resistance (KΩ) between contacts 4 b and 5 a of the lens motor plug.

7 > R > 2.5 (KΩ)

N — Check factor pot R 1. Check calibration.

Y

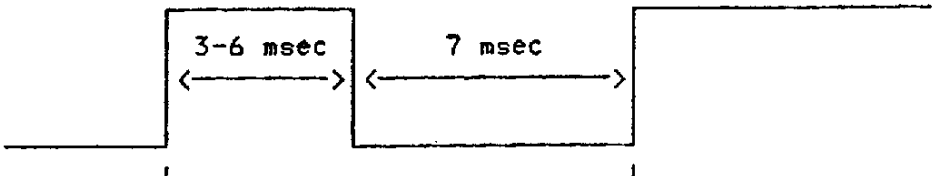
Reconnect lens plug X 6.

Press + hold the enter key. Power on.
Thus the testprogram is selected.

All following measurements take place on the power control PCB.

Press the enter key once. Measure the signal at V 6 / 3.

The unit exits the keyboard test and enters the potentiometer test



correct — N → Go to 5.6.

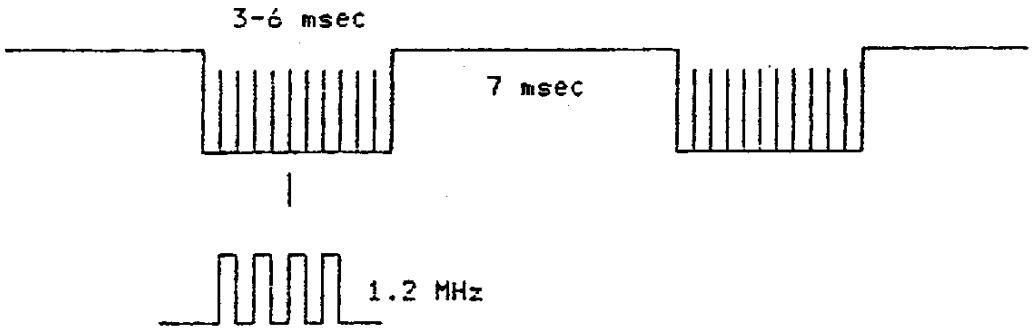
Y

Measure the frequency at V 15 / 1.

1.2 MHz — N → Check V 5, clock line.

Y

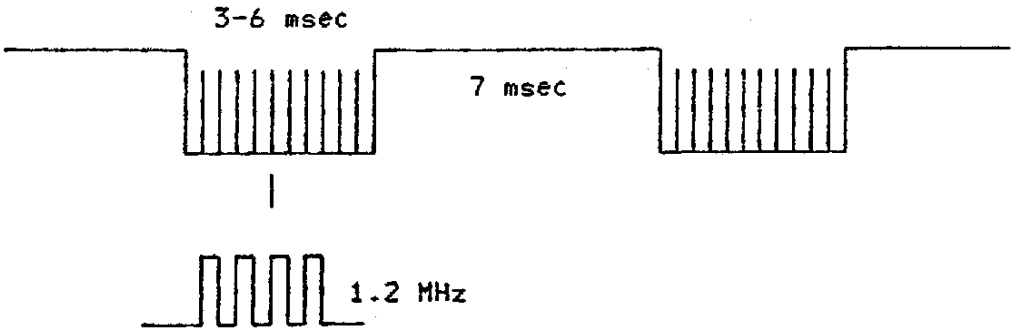
Measure the signal at V 15 / 3.



correct — N → Check V 15.

Y

Measure the signal at V 16 / 1.



correct — N → Go to 5.7.

Y

1. Power off. Disconnect lens motor plug X 6.
2. Connect the Z 80 test unit.
3. Address switches: 800C

1. Set mode sel. to run (TU). 2. Power on. 3. Press test (TU)

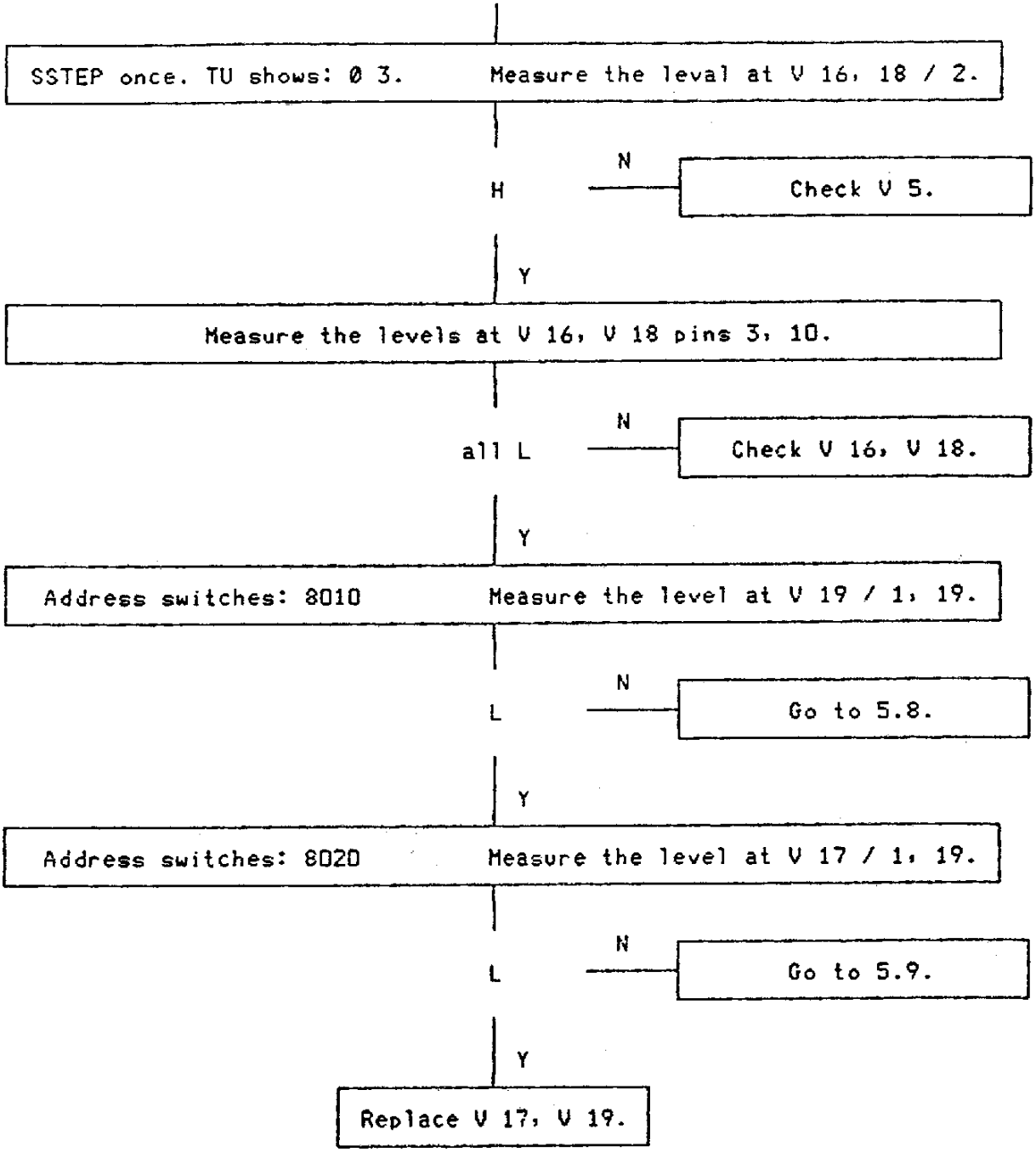
1. Set the mode sel. to ad. stop (TU).
2. Press the enter key. The TU shows: 800C 00.
3. Press SSTEP 2 times (TU). The TU shows: 800C 01.
Measure the frequencies at V 16, V 18.

V 16								
Pin	3	4	5	6	11	10	9	8
Period µsec								
micro sec.	1.67	3.3	6.6	13.3	26.6	53.3	10.6	31.3
V 18								
Pin	11	10	9	8	3	4		
Period msec								
milli sec.	0.43	0.85	1.7	3.4	6.8	13.6		

Y — correct

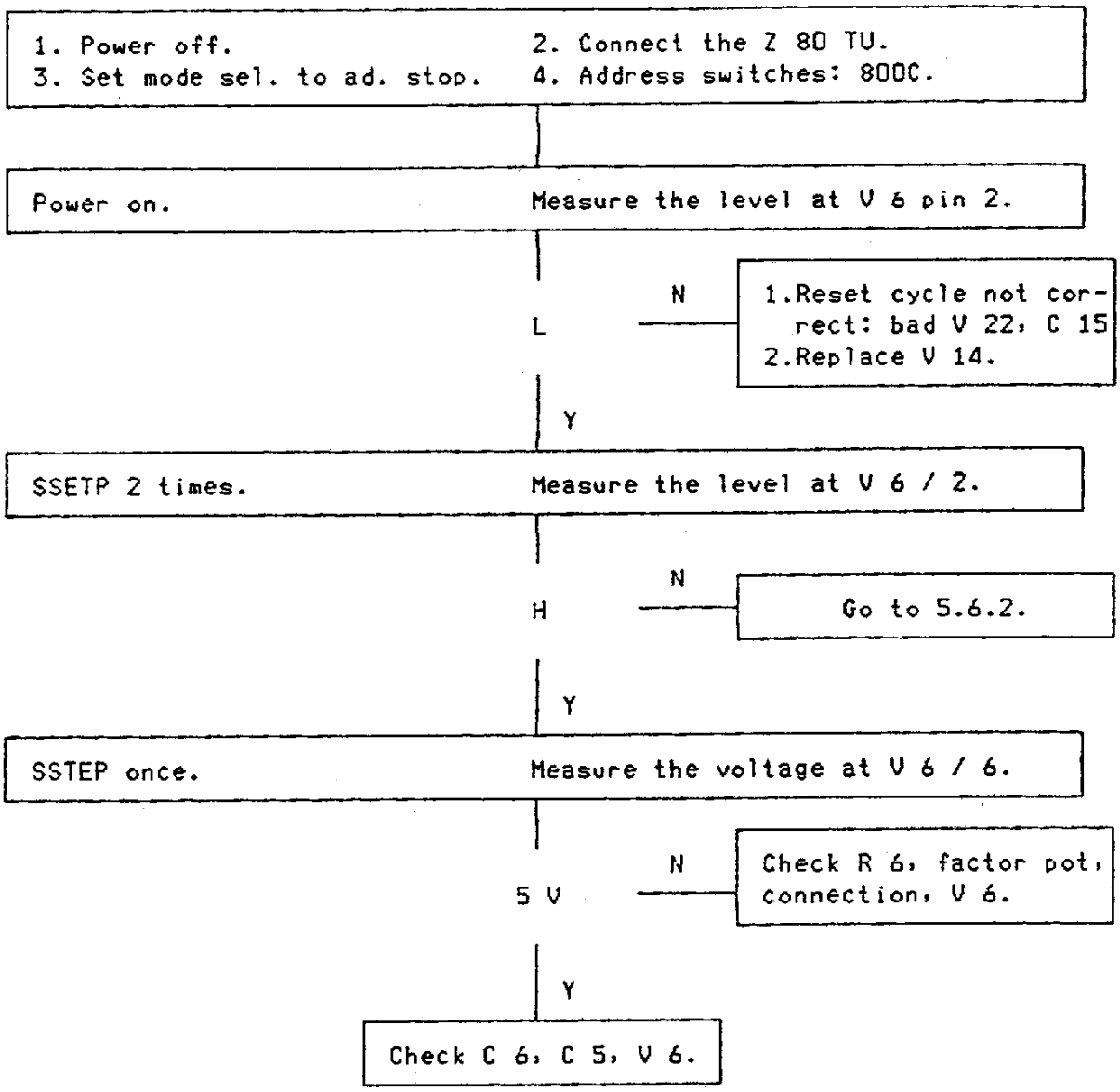
N

The clear (CL) input must be at L level. If it is H, replace V 5.
Else replace bad counter (V 16 or V 18).

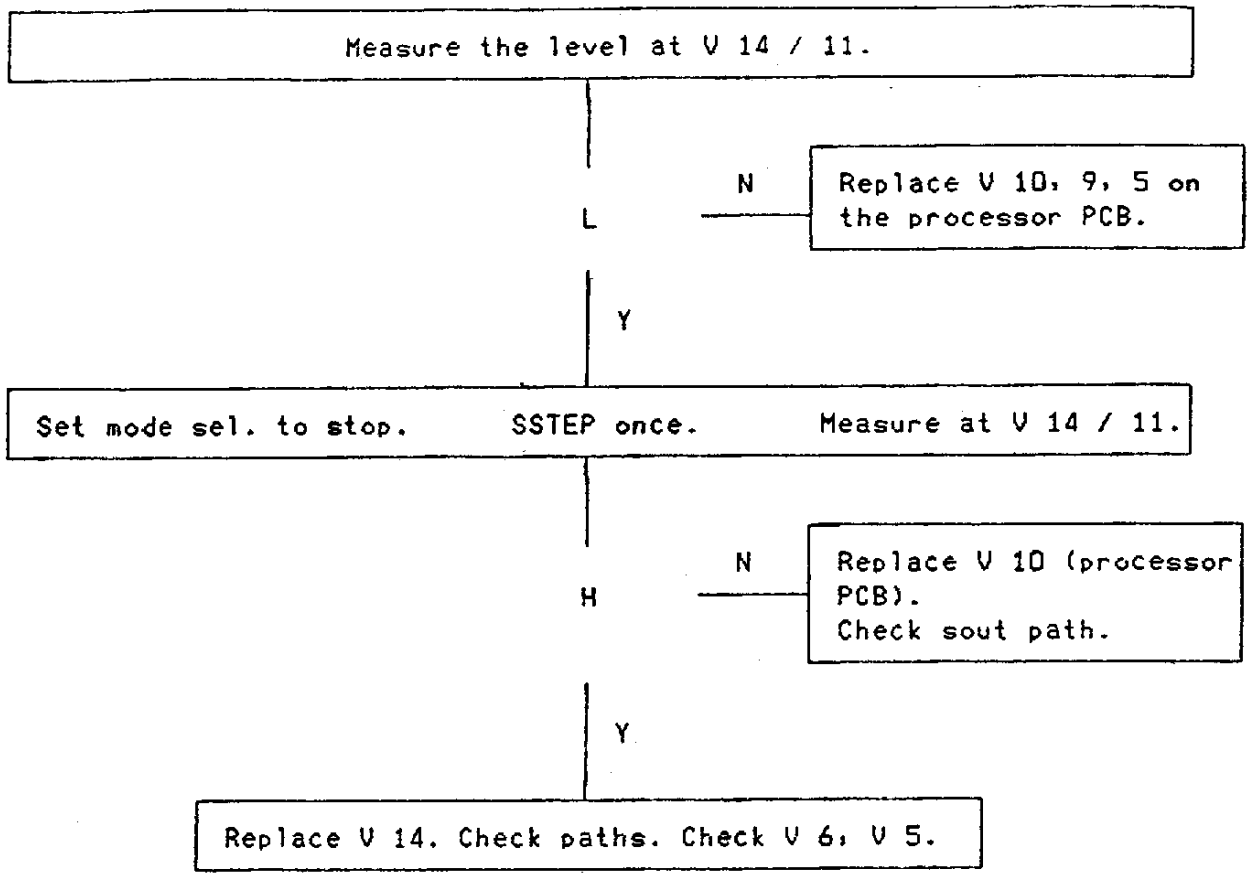

SSTEP once. TU shows: 0 3.
Measure the leval at V 16, 18 / 2.
H
N
Check V 5.
Y
Measure the levels at V 16, V 18 pins 3, 10.
all L
N
Check V 16, V 18.
Y
Address switches: 8010
Measure the level at V 19 / 1, 19.
L
N
Go to 5.8.
Y
Address switches: 8020
Measure the level at V 17 / 1, 19.
L
N
Go to 5.9.
Y
Replace V 17, V 19.

FAILURE CHART 5.6

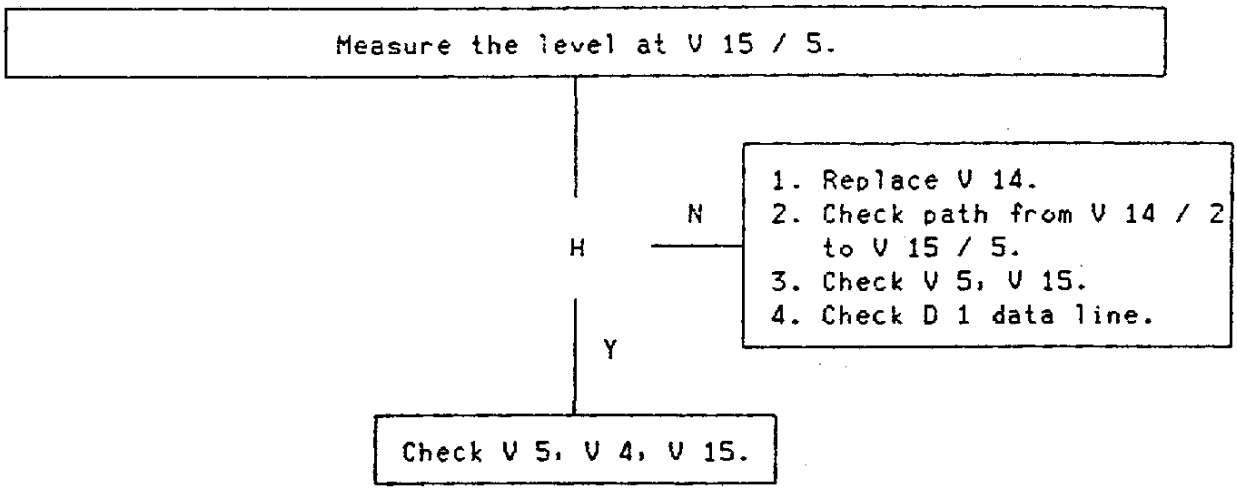
All measuring takes place on the power control PCB.



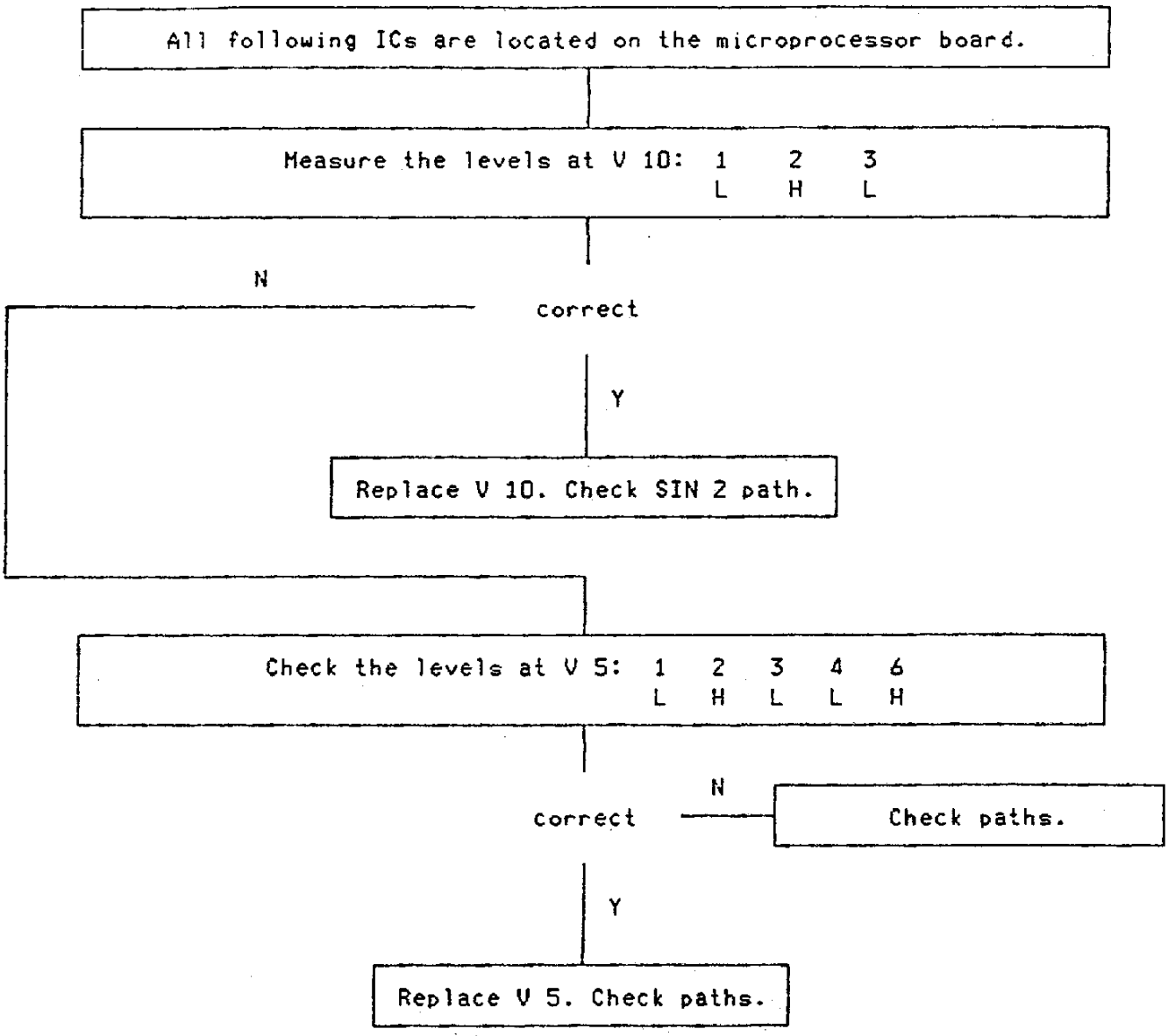
All measuring takes place on the power control PCB.



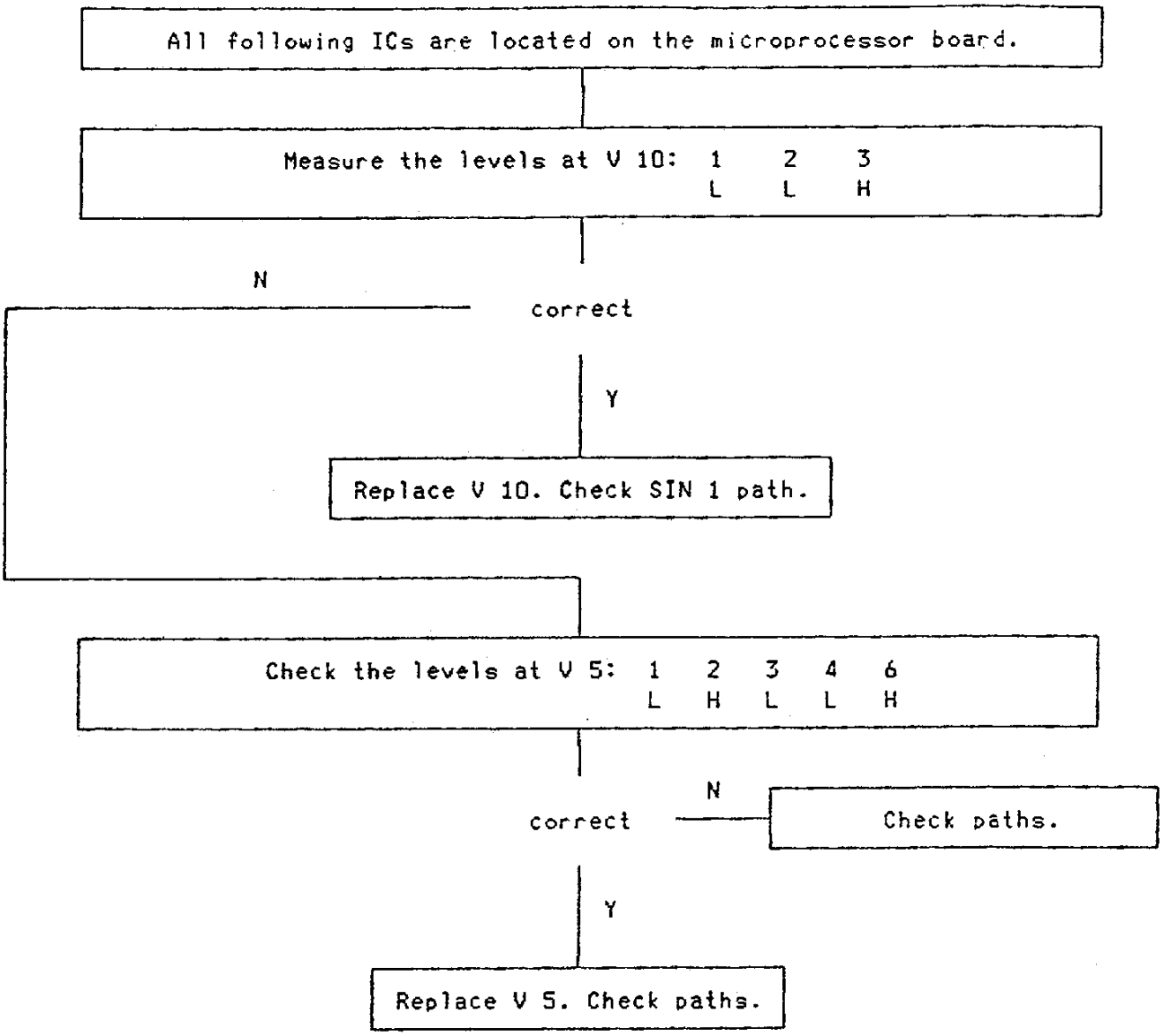
FAILURE CHART 5.7



FAILURE CHART 5.8



FAILURE CHART 5.9



AF - MODULE TEST

Press and hold the enter key. Power on.
Press enter: display.
Press the "up" or "down" key and the "-" key.
Measure the signal at V 15 / 9 on the power control interface PCB.

correct — N → Go to 5.B

Y

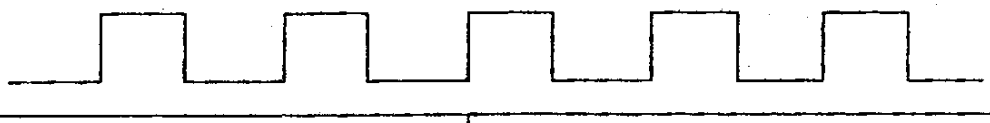
Measure at V 15 / 11.

correct — N → Go to 5.C

Y

Go to 5.5.3 to check counter.

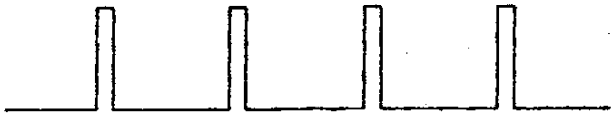
Press the "up" or "down" and the "-" key.
The lens must move in fast speed.
Measure the signal at V 9 / + C (see layout schematics) on the lens motor PCB.



correct — N → Check V 9.

Y

Measure the signal at V 7 / 3.

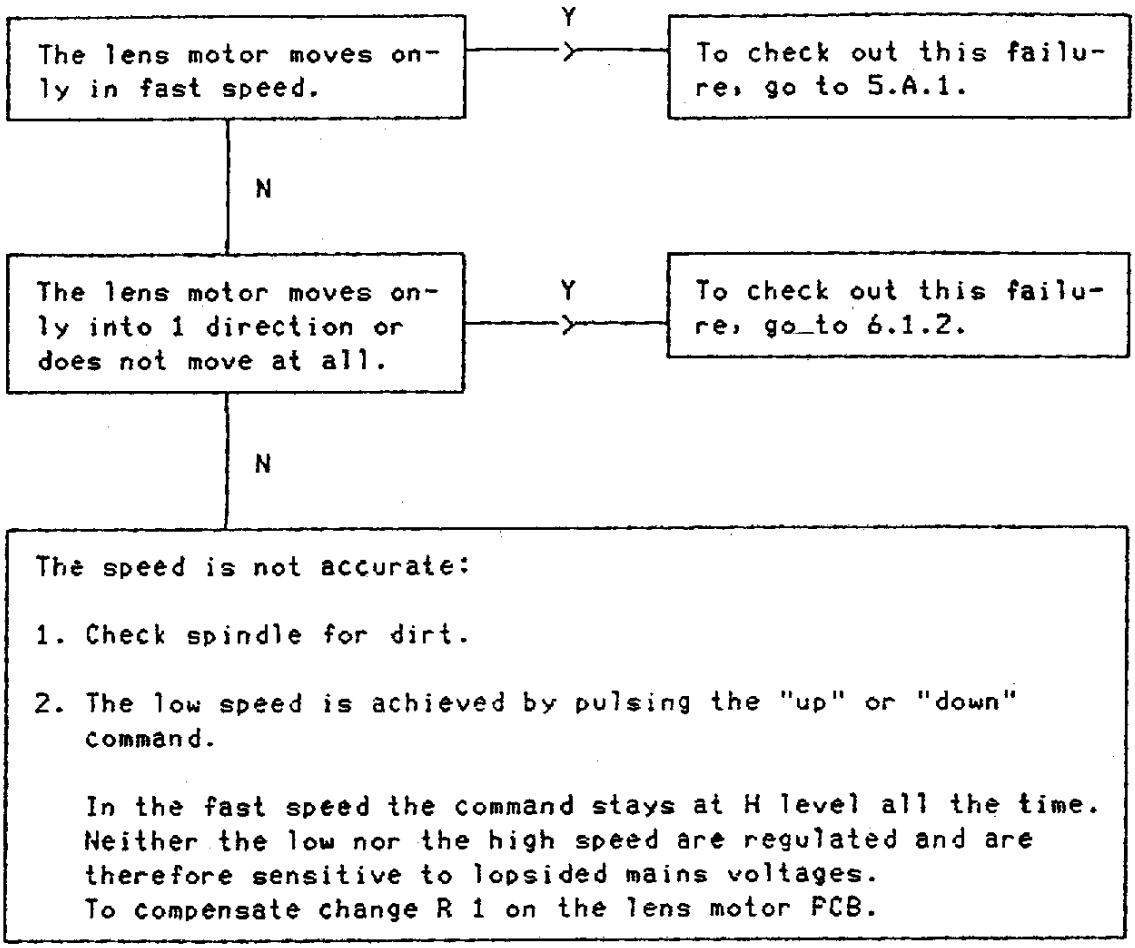


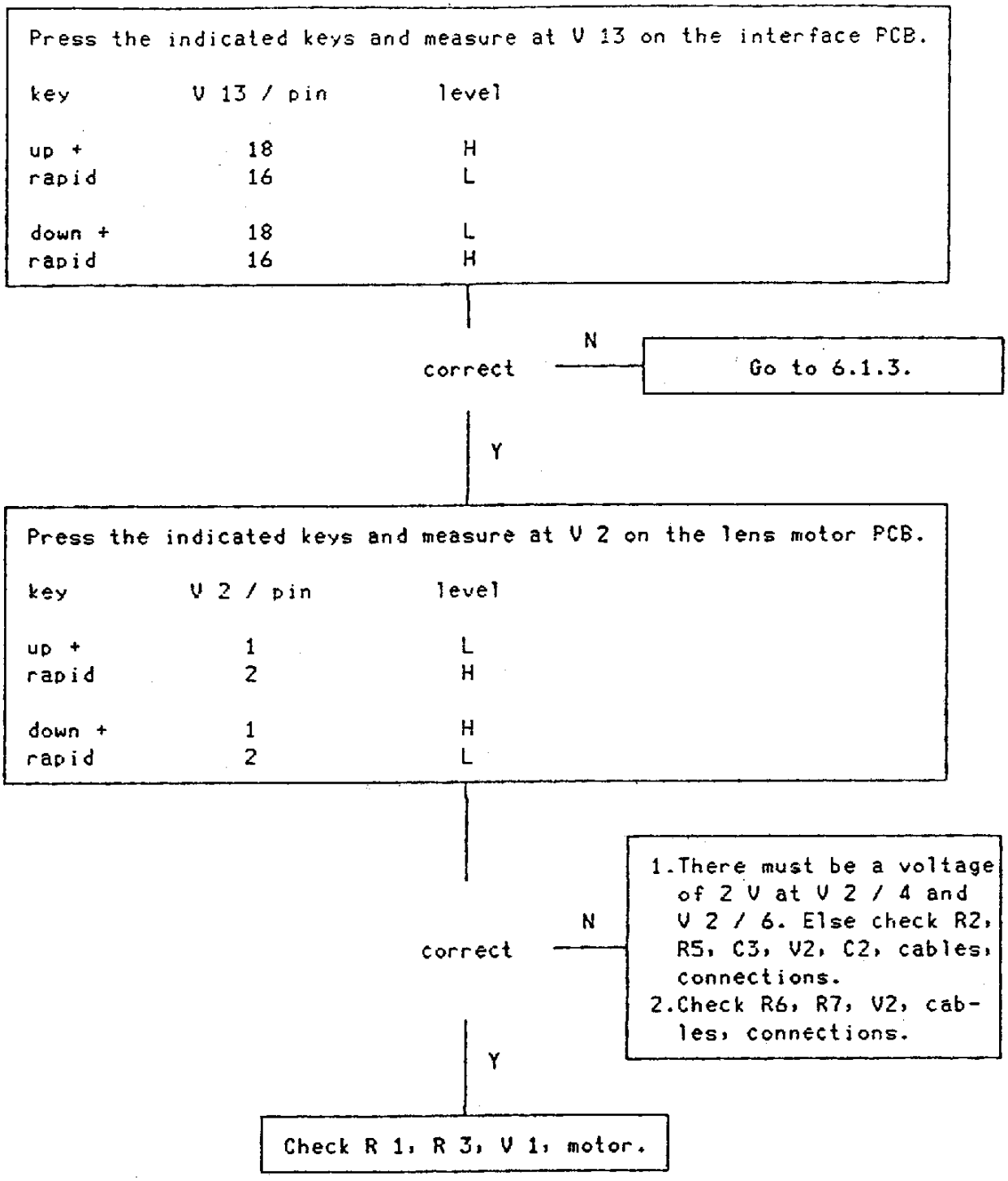
correct — N → Replace V 2, V 7, V 8.

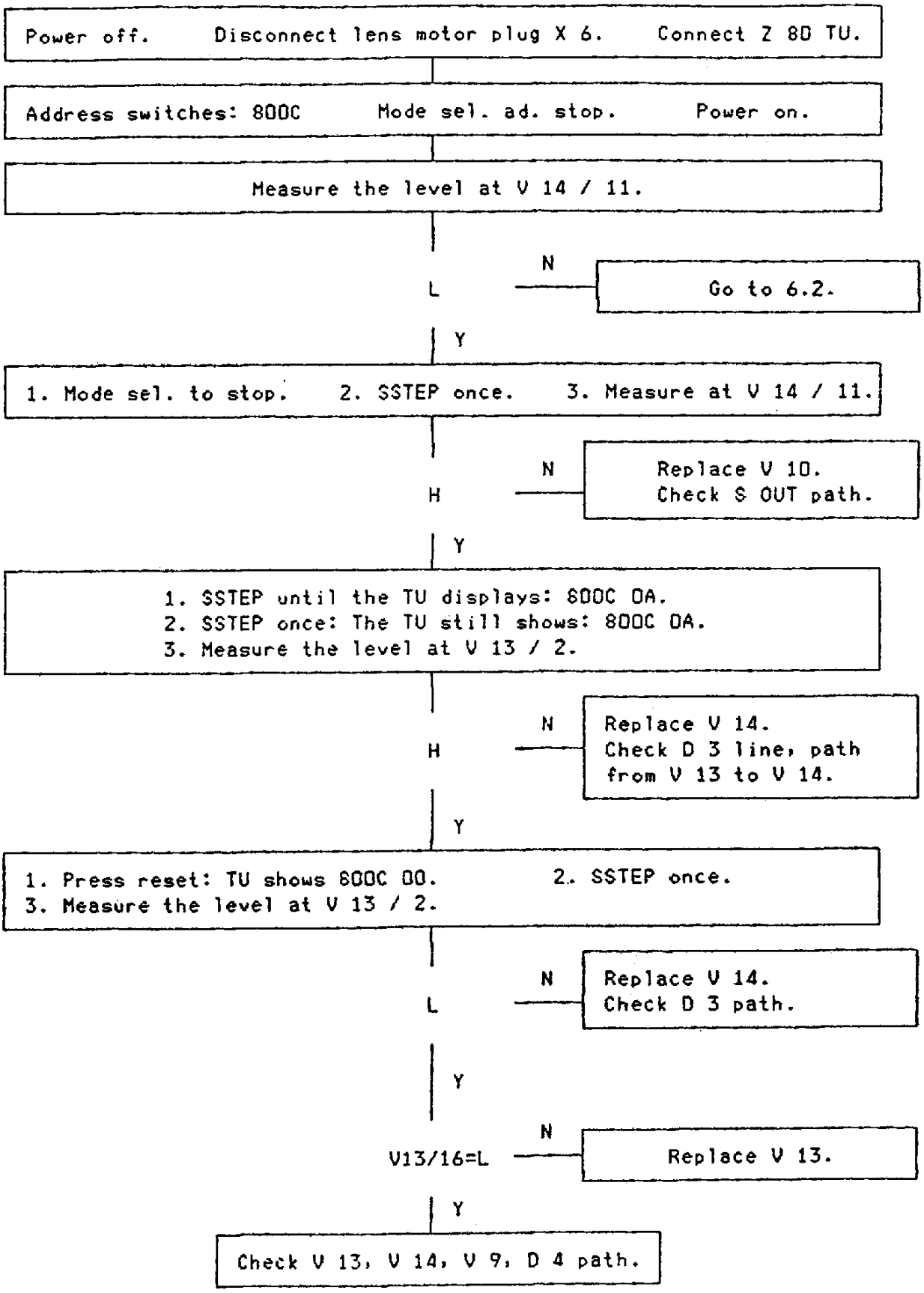
Y

Check R 8, cables.
Check R 5, V 4, V 5 on the interface PCB.

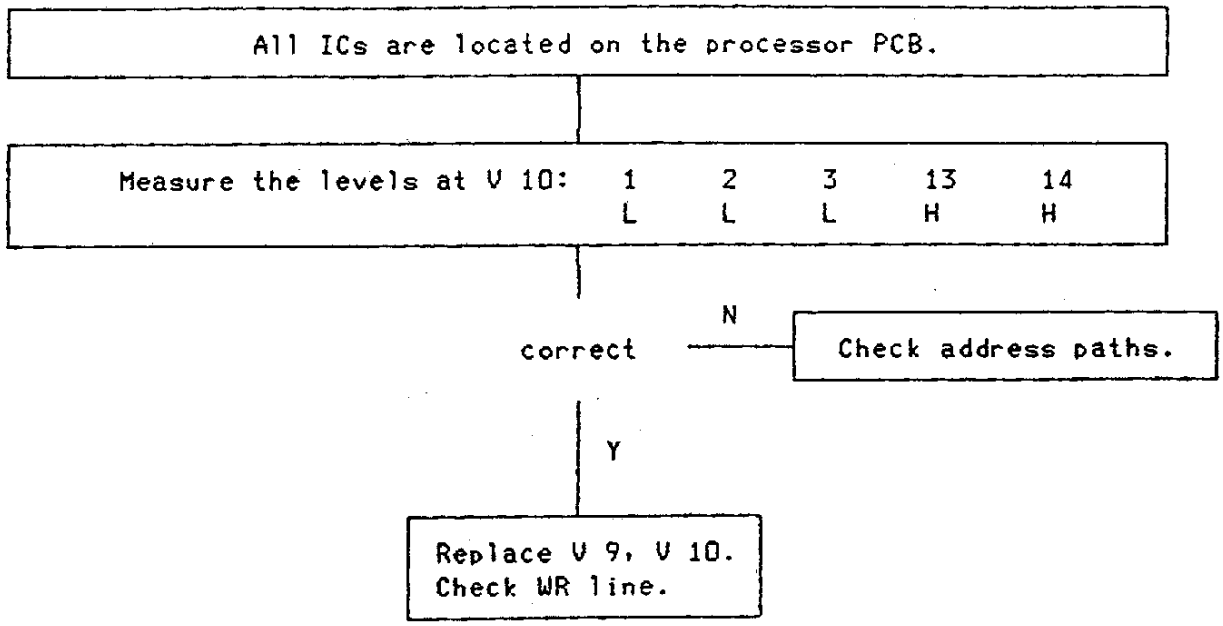
Following failures are possible:




Press the indicated keys and measure at V 13 on the interface PCB.
key V 13 / pin level
up + 18 H
rapid 16 L
down + 18 L
rapid 16 H
correct
N
Go to 6.1.3.
Y
Press the indicated keys and measure at V 2 on the lens motor PCB.
key V 2 / pin level
up + 1 L
rapid 2 H
down + 1 H
rapid 2 L
correct
N
1.There must be a voltage of 2 V at V 2 / 4 and V 2 / 6. Else check R2, R5, C3, V2, C2, cables, connections.
2.Check R6, R7, V2, cables, connections.
Y
Check R 1, R 3, V 1, motor.

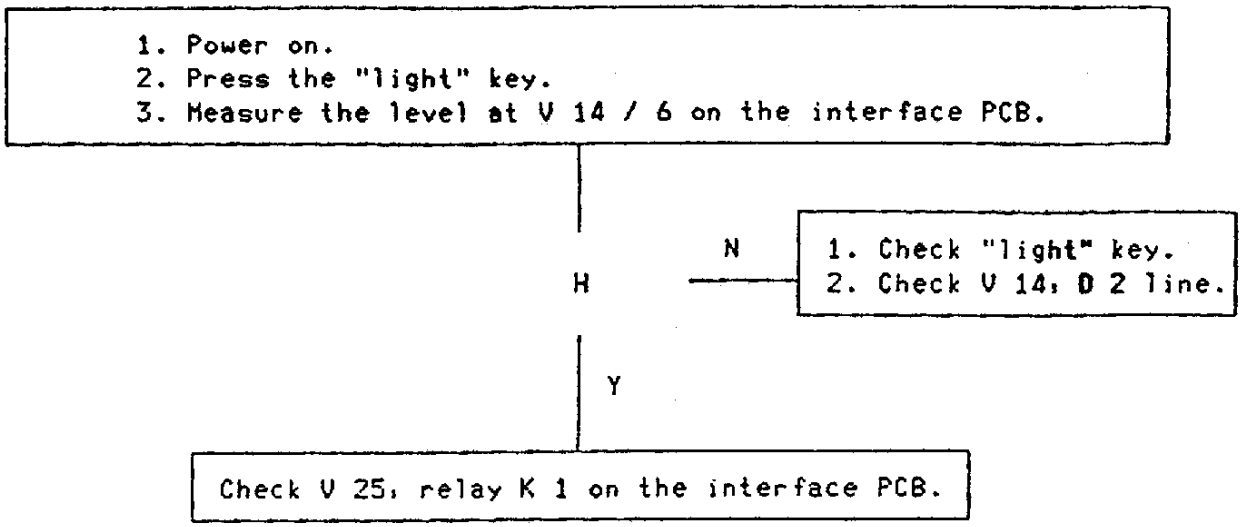

Power off. Disconnect lens motor plug X 6. Connect Z 80 TU.
Address switches: 800C Mode sel. ad. stop. Power on.
Measure the level at V 14 / 11.
L
N
Go to 6.2.
Y
1. Mode sel. to stop. 2. SSTEP once. 3. Measure at V 14 / 11.
H
N
Replace V 10.
Check S OUT path.
Y
1. SSTEP until the TU displays: 800C 0A.
2. SSTEP once: The TU still shows: 800C 0A.
3. Measure the level at V 13 / 2.
H
N
Replace V 14.
Check D 3 line, path
from V 13 to V 14.
Y
1. Press reset: TU shows 800C 00. 2. SSTEP once.
3. Measure the level at V 13 / 2.
L
N
Replace V 14.
Check D 3 path.
Y
V13/16=L
N
Replace V 13.
Y
Check V 13, V 14, V 9, D 4 path.

FAILURE CHART 6.2



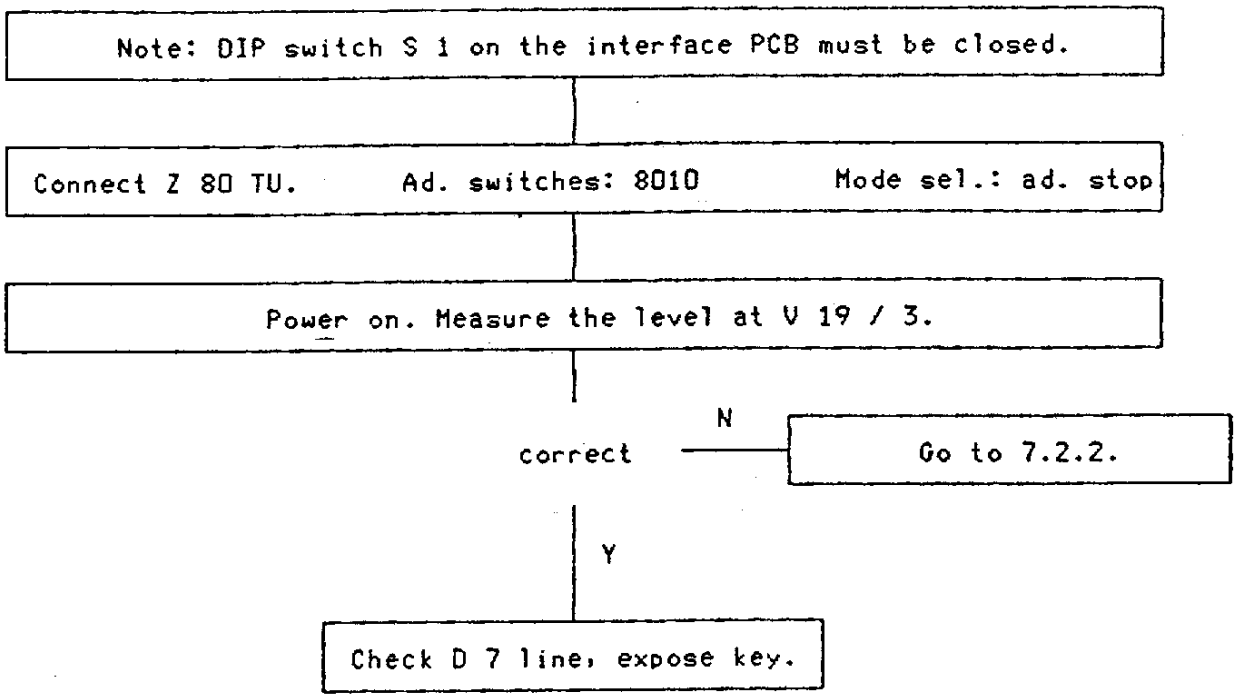
7.1 ELITE 2000 TIM: Lamp relay failure

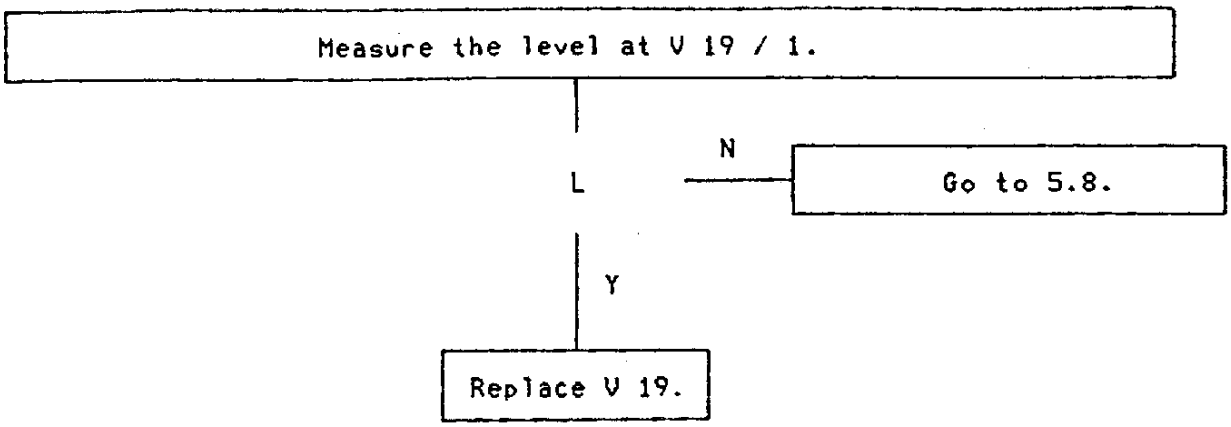
LAMP RELAY CHECK (with 2000 TIM only)



7.2 ELITE 2000 TIM: Timer failure

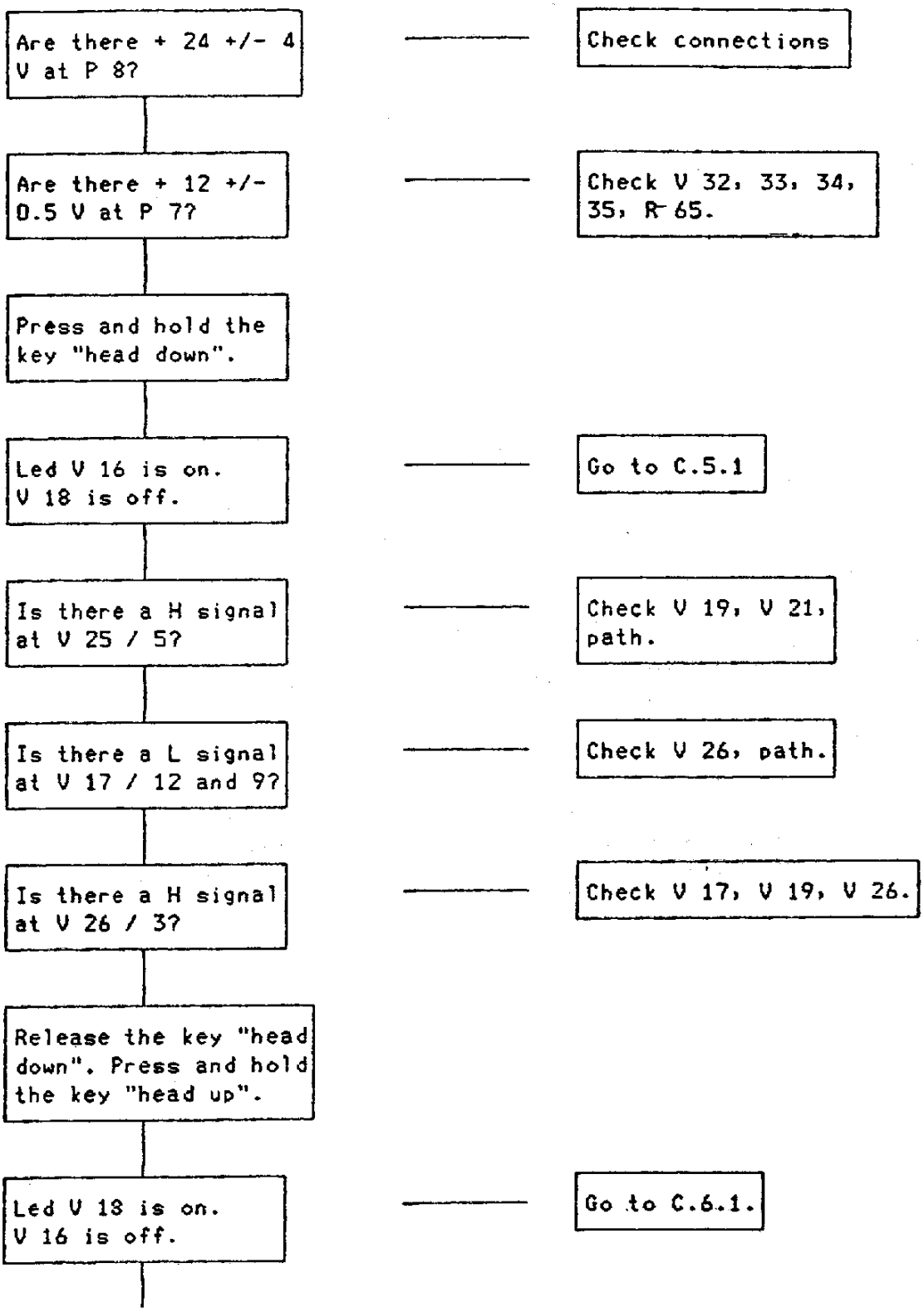
TIMER CHECK (with 2000 TIM only)

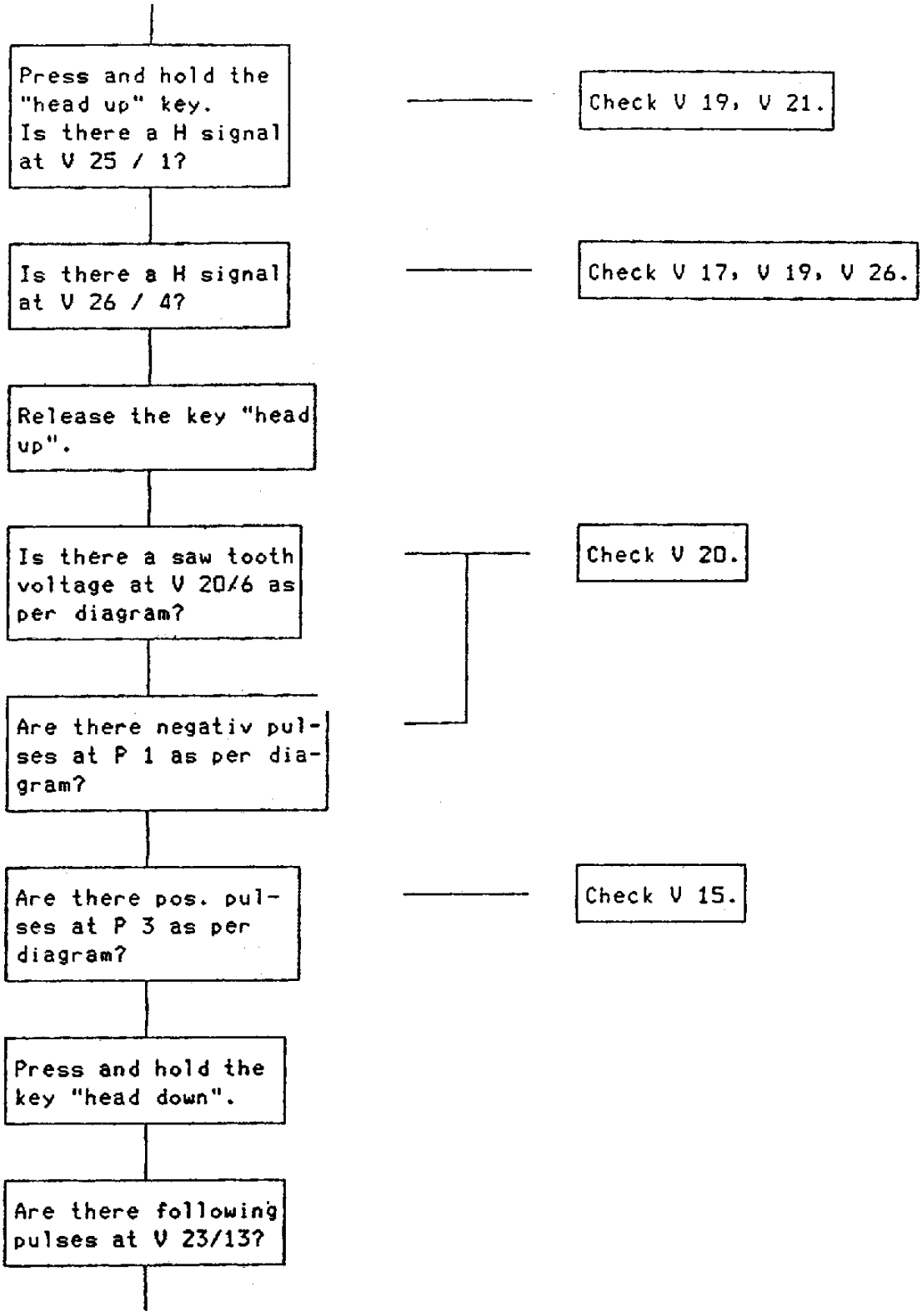


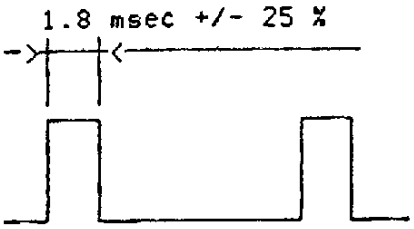

Measure the level at V 19 / 1.
L
N
Go to 5.8.
Y
Replace V 19.

C.0 ELITE 2000 MOT: Head movement failure

Possible faults:	flowcharts
The head stage cannot be moved at all	C.1.1
The head stage can only be raised	C.2.1
The head stage can only be lowered	C.7.1
The head moves only with high speed (or low speed is not correct and cannot be adjusted)	C.3.1
The head moves only with low speed	C.3.1


Are there + 24 +/- 4 V at P 8?
Check connections
Are there + 12 +/- 0.5 V at P 7?
Check V 32, 33, 34, 35, R 65.
Press and hold the key "head down".
Led V 16 is on. V 18 is off.
Go to C.5.1
Is there a H signal at V 25 / 5?
Check V 19, V 21, path.
Is there a L signal at V 17 / 12 and 9?
Check V 26, path.
Is there a H signal at V 26 / 3?
Check V 17, V 19, V 26.
Release the key "head down". Press and hold the key "head up".
Led V 18 is on. V 16 is off.
Go to C.6.1.

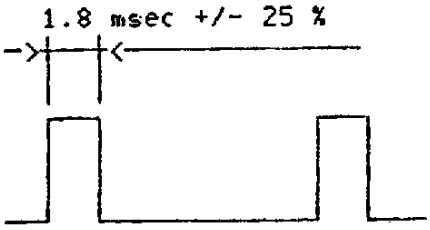

Press and hold the "head up" key. Is there a H signal at V 25 / 1?
Check V 19, V 21.
Is there a H signal at V 26 / 4?
Check V 17, V 19, V 26.
Release the key "head up".
Is there a saw tooth voltage at V 20/6 as per diagram?
Check V 20.
Are there negativ pulses at P 1 as per diagram?
Are there pos. pulses at P 3 as per diagram?
Check V 15.
Press and hold the key "head down".
Are there following pulses at V 23/13?



Check V 25, 15.

Release the key "head down". Press and hold the key "head up".

Are there following pulses at V 23/5?



Check V 25.

Release the key "head up".

Is there an H signal at P 2?

Check V 36, V 42 and motor. resp. setting of trimmer R 67.

Is there an H signal at V 21/11?

Check V 21.

Is there a L signal at V 10 / 8?

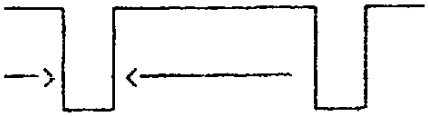
— Go to C.4.3.

Press and hold the key "head down".

Are there +2 V at P 4?

— Check V 24 resp. setting of trimmer R 46 (min. speed).

Are there following pulses at P 6?



— Check V 24.

1 to 5 msec.

Are the same pulses, inverted, at V 25/4?

— Check V 10, V 25.

Release the key "head down". Press and hold the key "head up".

Are the same pulses at V 25/3?

— Check V 10, V 25.

The faults are at V 27, V 29, V 37, V 40, V 45, V 46, V 47, V 48, V 49, V 50.

Press + hold the "head down" key. Lead V 16 must come on.
Led V 18 must be off.

correct — N → Go to C.5.1.

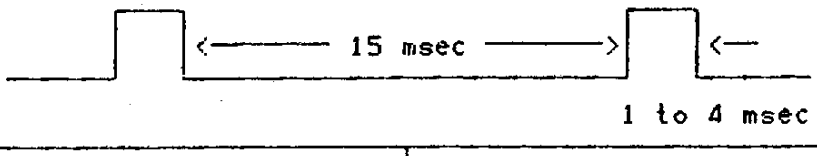
Y

Press and hold the "head down" key.

V25/5=H — N → Check V 19, 21

Y

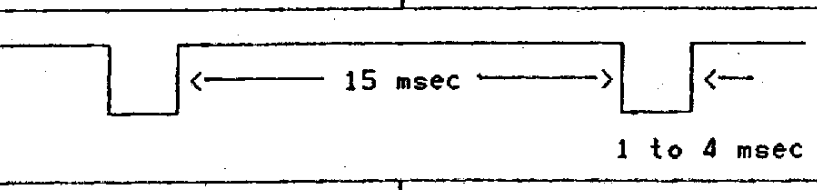
Press and hold the "head down" key.
Measure the signal at V 25 / 4.



correct — N → Go to C.2.4.

Y

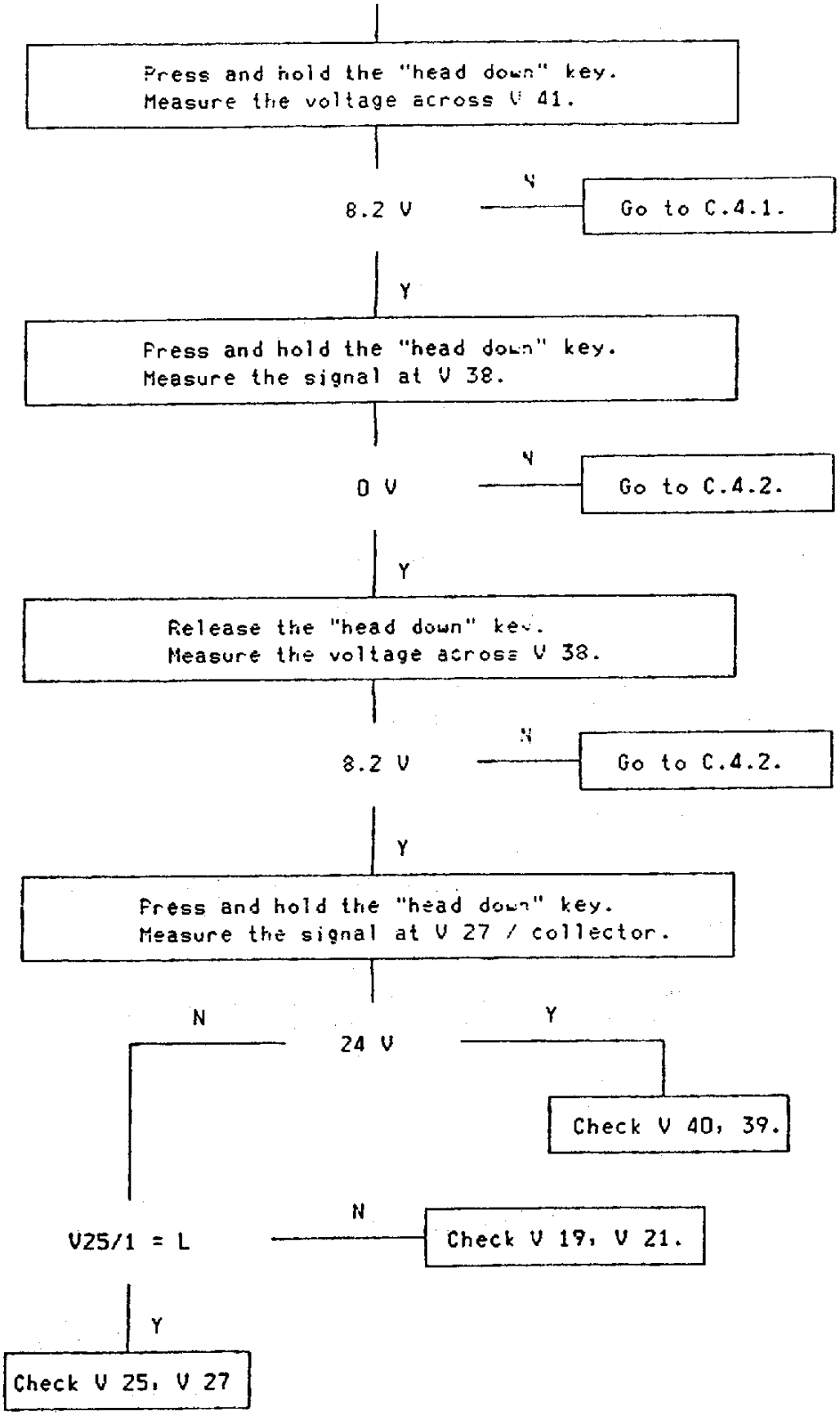
Measure the signal at V 29 / collector.

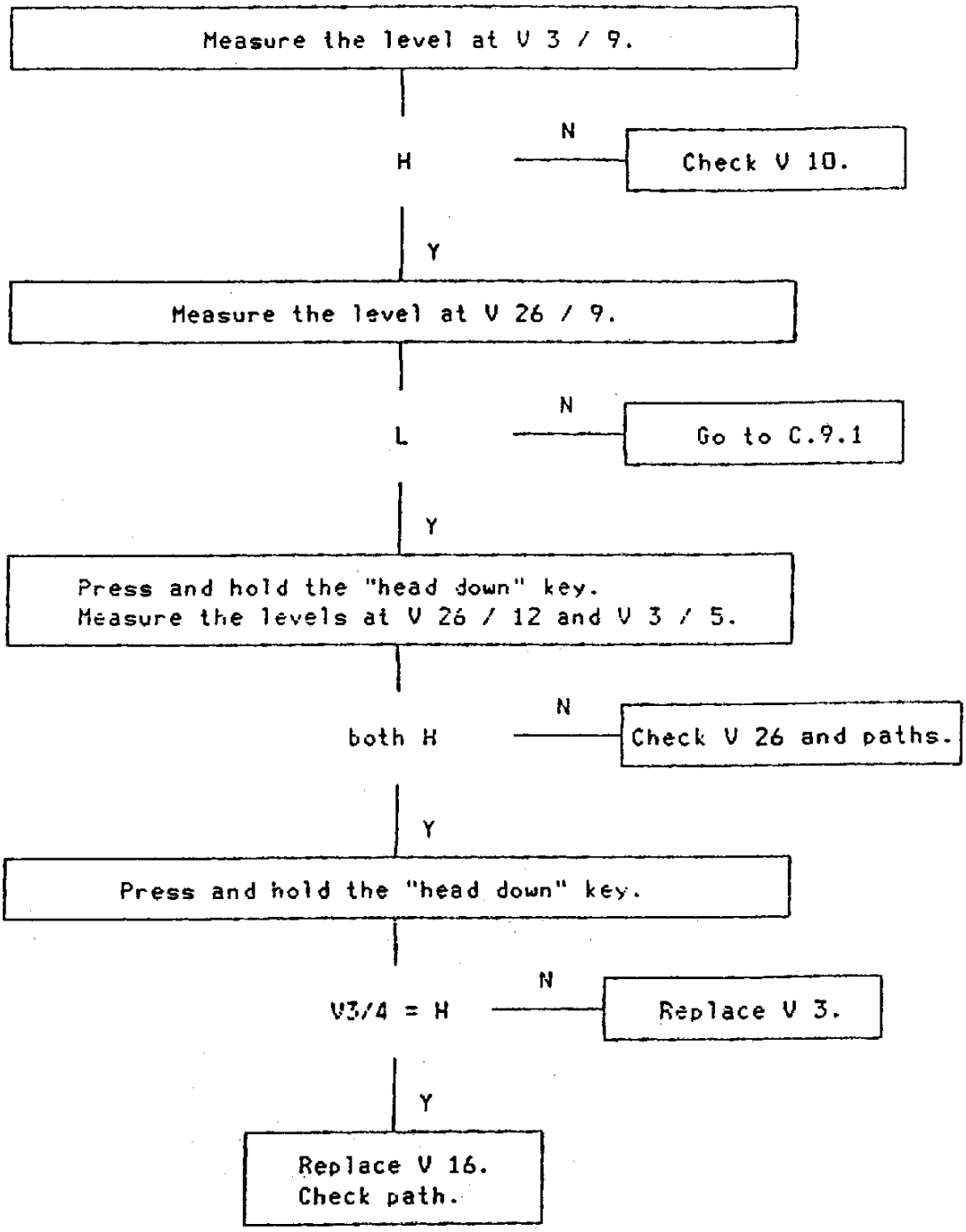


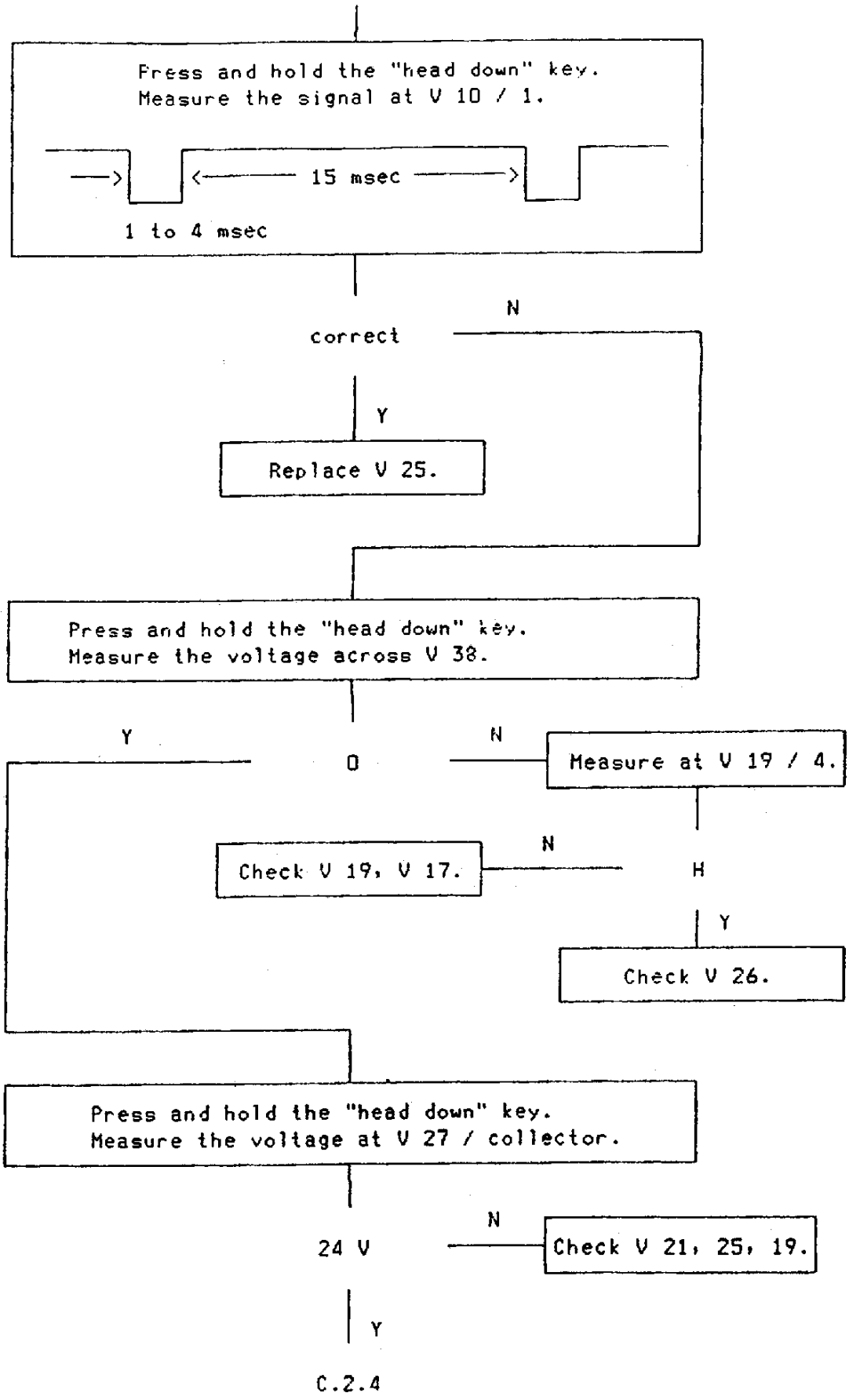
correct — N → Replace V 29. Check R 56, 66, path.

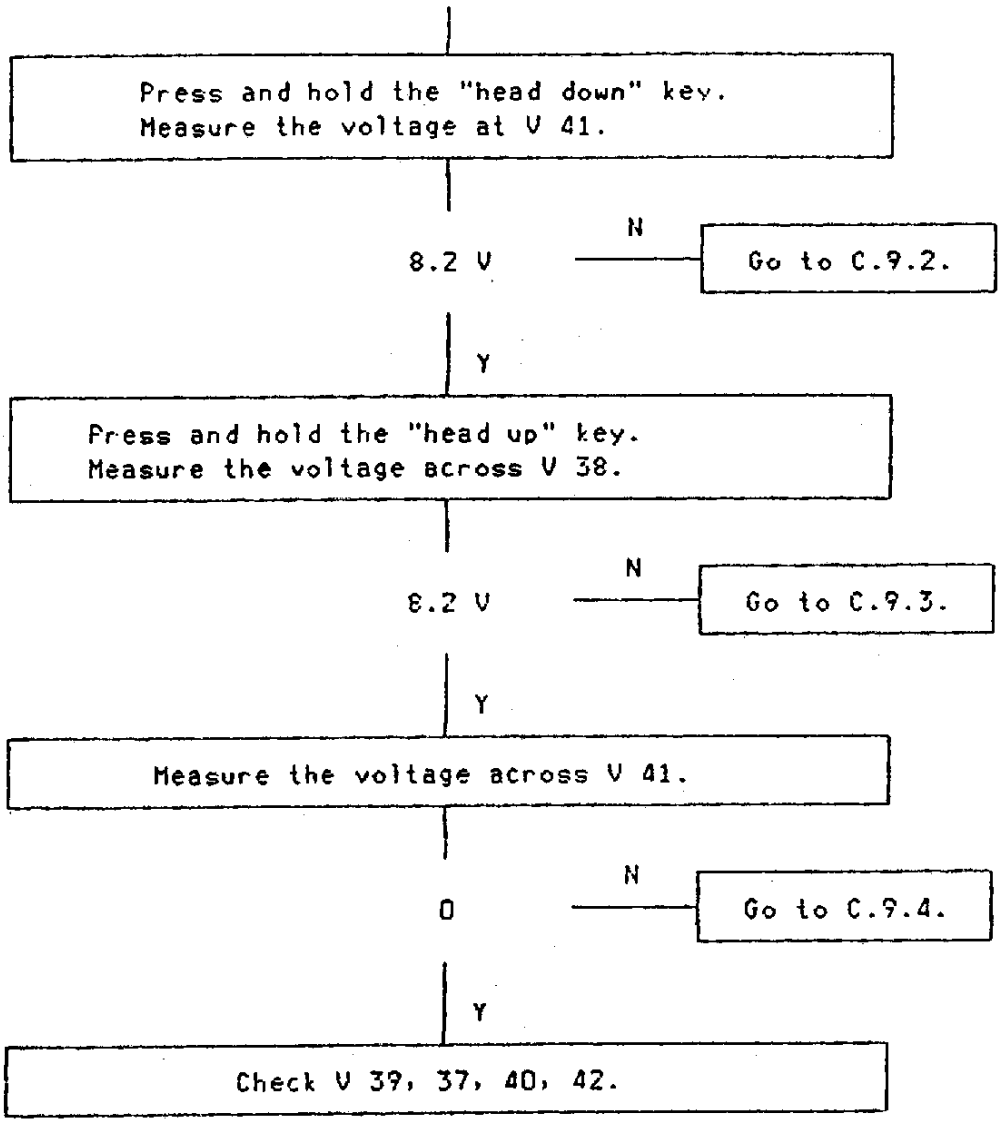
Y

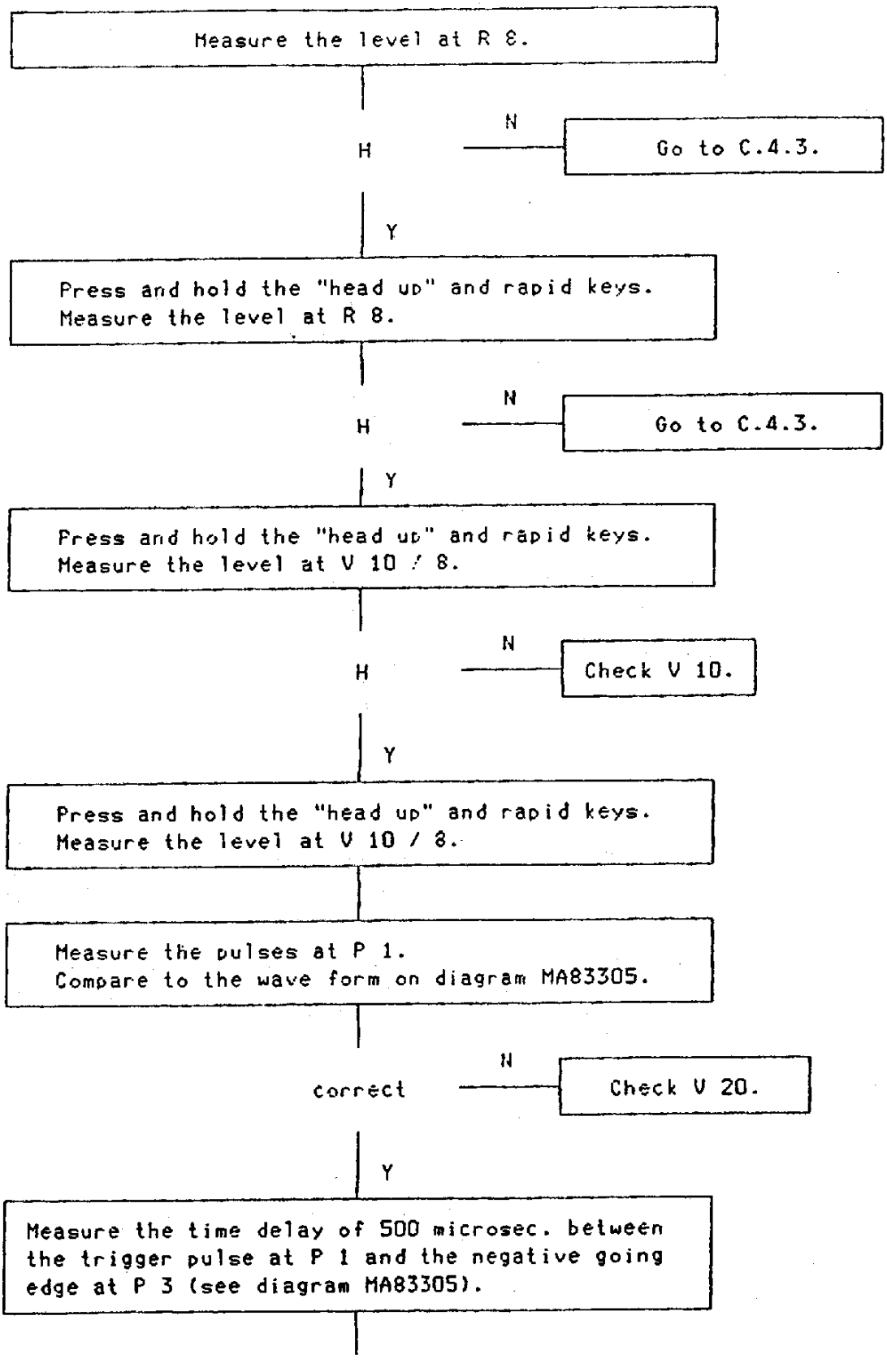
C.2.1

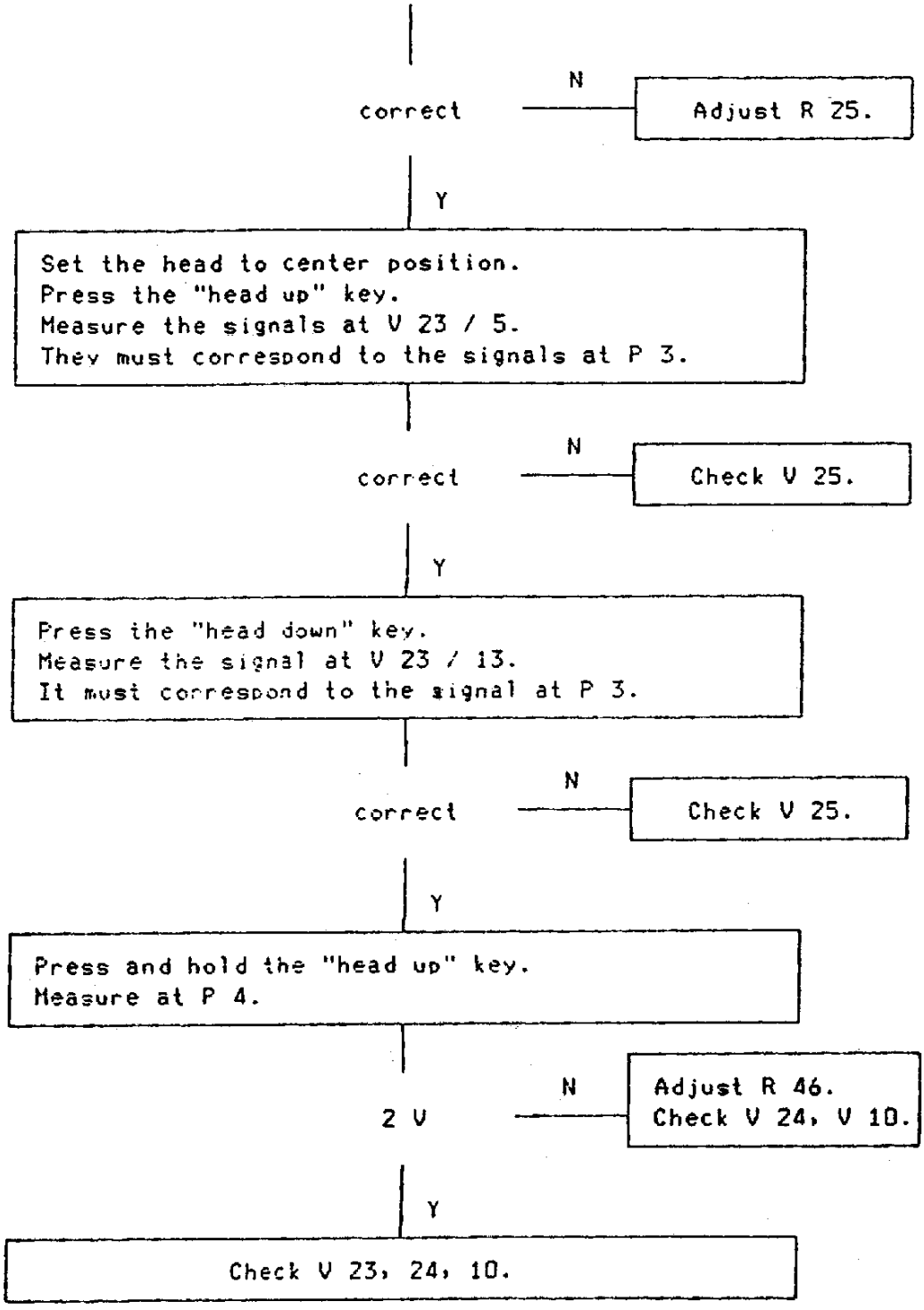

Press and hold the "head down" key.
Measure the voltage across V 41.
8.2 V
N
Go to C.4.1.
Y
Press and hold the "head down" key.
Measure the signal at V 38.
0 V
N
Go to C.4.2.
Y
Release the "head down" key.
Measure the voltage across V 38.
8.2 V
N
Go to C.4.2.
Y
Press and hold the "head down" key.
Measure the signal at V 27 / collector.
N
24 V
Y
Check V 40, 39.
V25/1 = L
N
Check V 19, V 21.
Y
Check V 25, V 27


Measure the level at V 3 / 9.
H
N
Check V 10.
Y
Measure the level at V 26 / 9.
L
N
Go to C.9.1
Y
Press and hold the "head down" key.
Measure the levels at V 26 / 12 and V 3 / 5.
both H
N
Check V 26 and paths.
Y
Press and hold the "head down" key.
V3/4 = H
N
Replace V 3.
Y
Replace V 16.
Check path.

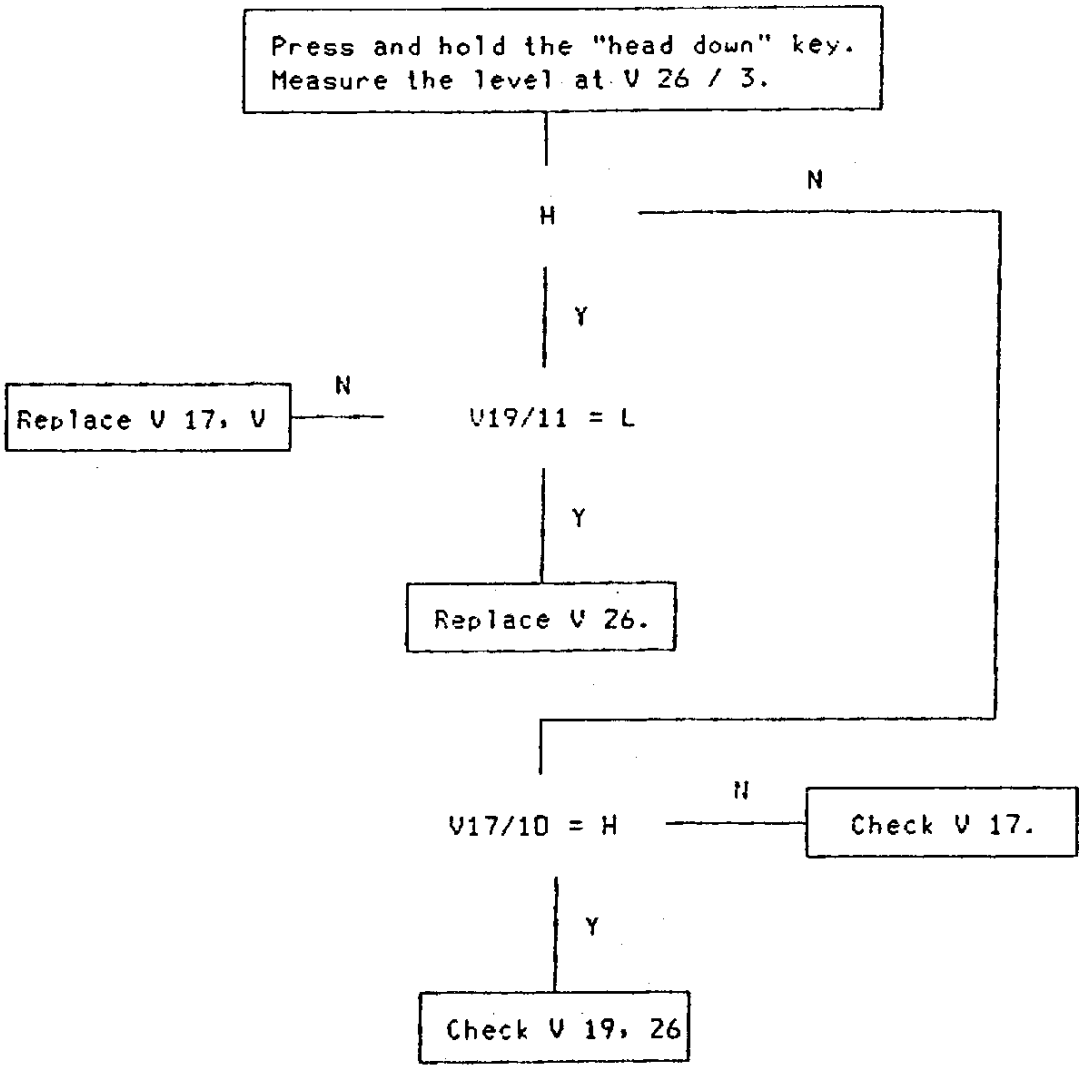

Press and hold the "head down" key.
Measure the signal at V 10 / 1.
15 msec
1 to 4 msec
correct
N
Y
Replace V 25.
Press and hold the "head down" key.
Measure the voltage across V 38.
Y
0
N
Measure at V 19 / 4.
Check V 19, V 17.
N
H
Y
Check V 26.
Press and hold the "head down" key.
Measure the voltage at V 27 / collector.
24 V
N
Check V 21, 25, 19.
Y

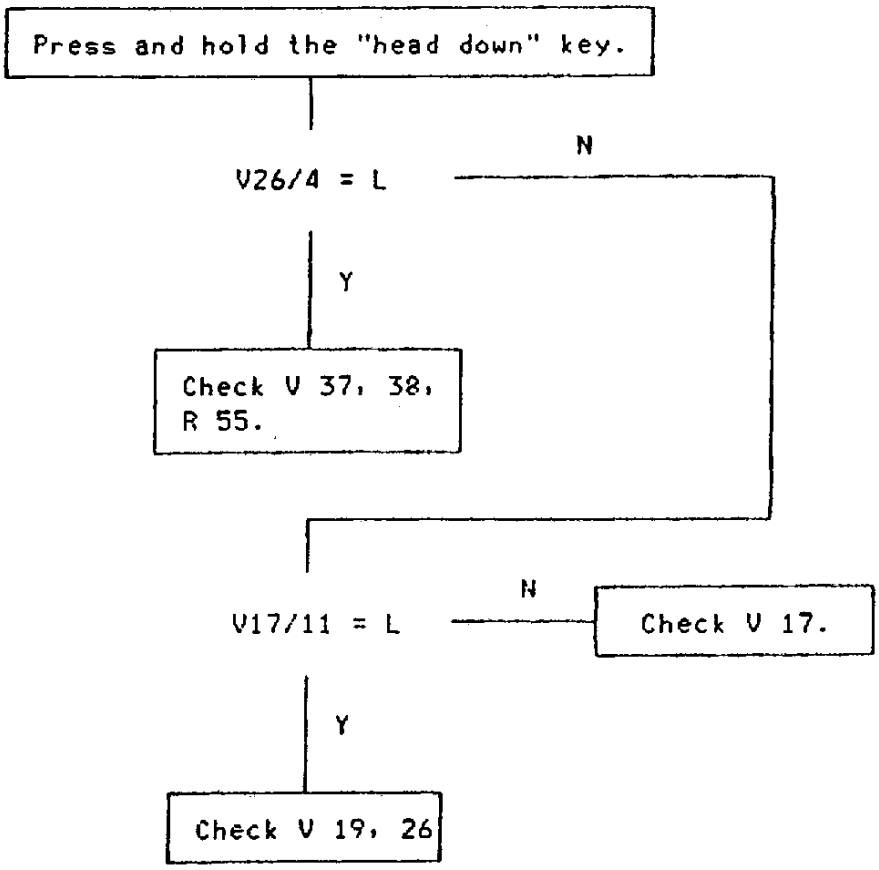

Press and hold the "head down" key.
Measure the voltage at V 41.
8.2 V
N
Go to C.9.2.
Y
Press and hold the "head up" key.
Measure the voltage across V 38.
8.2 V
N
Go to C.9.3.
Y
Measure the voltage across V 41.
0
N
Go to C.9.4.
Y
Check V 39, 37, 40, 42.

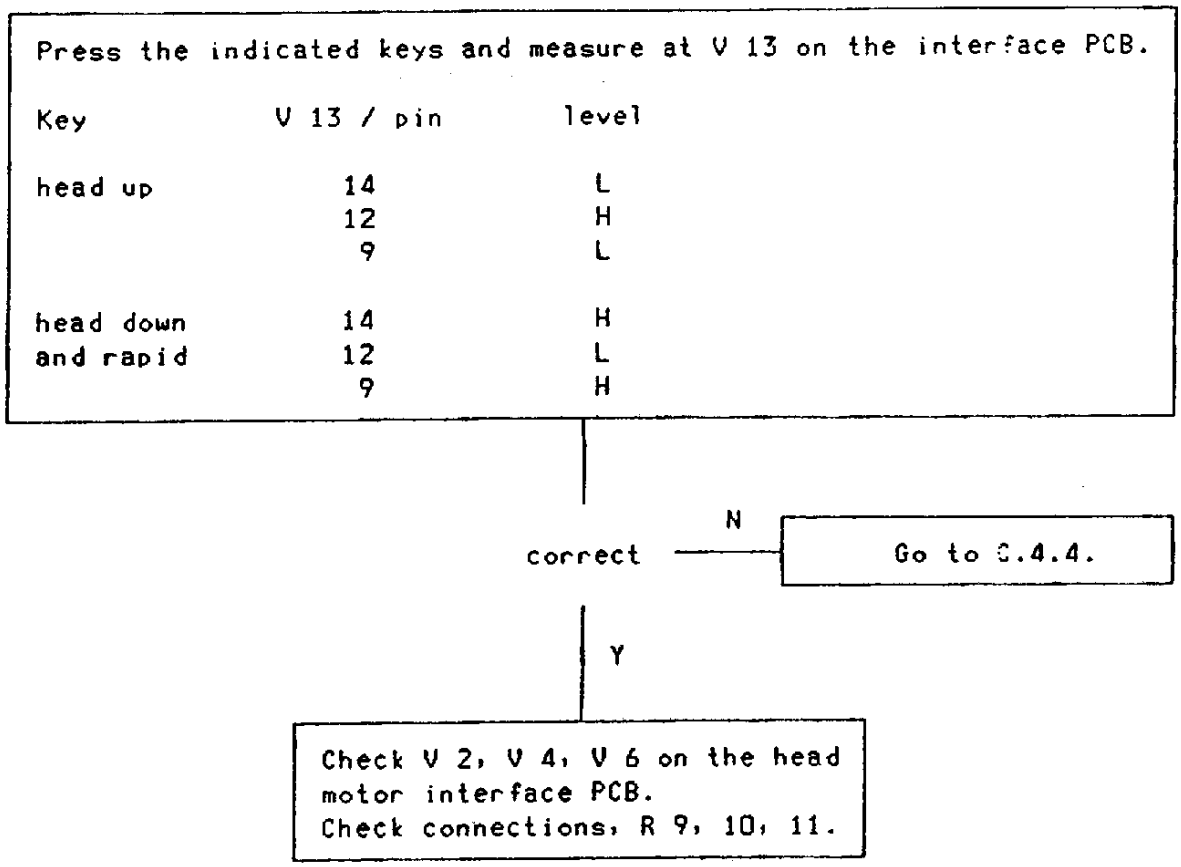

Measure the level at R 8.
H
N
Go to C.4.3.
Y
Press and hold the "head up" and rapid keys.
Measure the level at R 8.
H
N
Go to C.4.3.
Y
Press and hold the "head up" and rapid keys.
Measure the level at V 10 / 8.
H
N
Check V 10.
Y
Press and hold the "head up" and rapid keys.
Measure the level at V 10 / 8.
Measure the pulses at P 1.
Compare to the wave form on diagram MA83305.
correct
N
Check V 20.
Y
Measure the time delay of 500 microsec. between the trigger pulse at P 1 and the negative going edge at P 3 (see diagram MA83305).

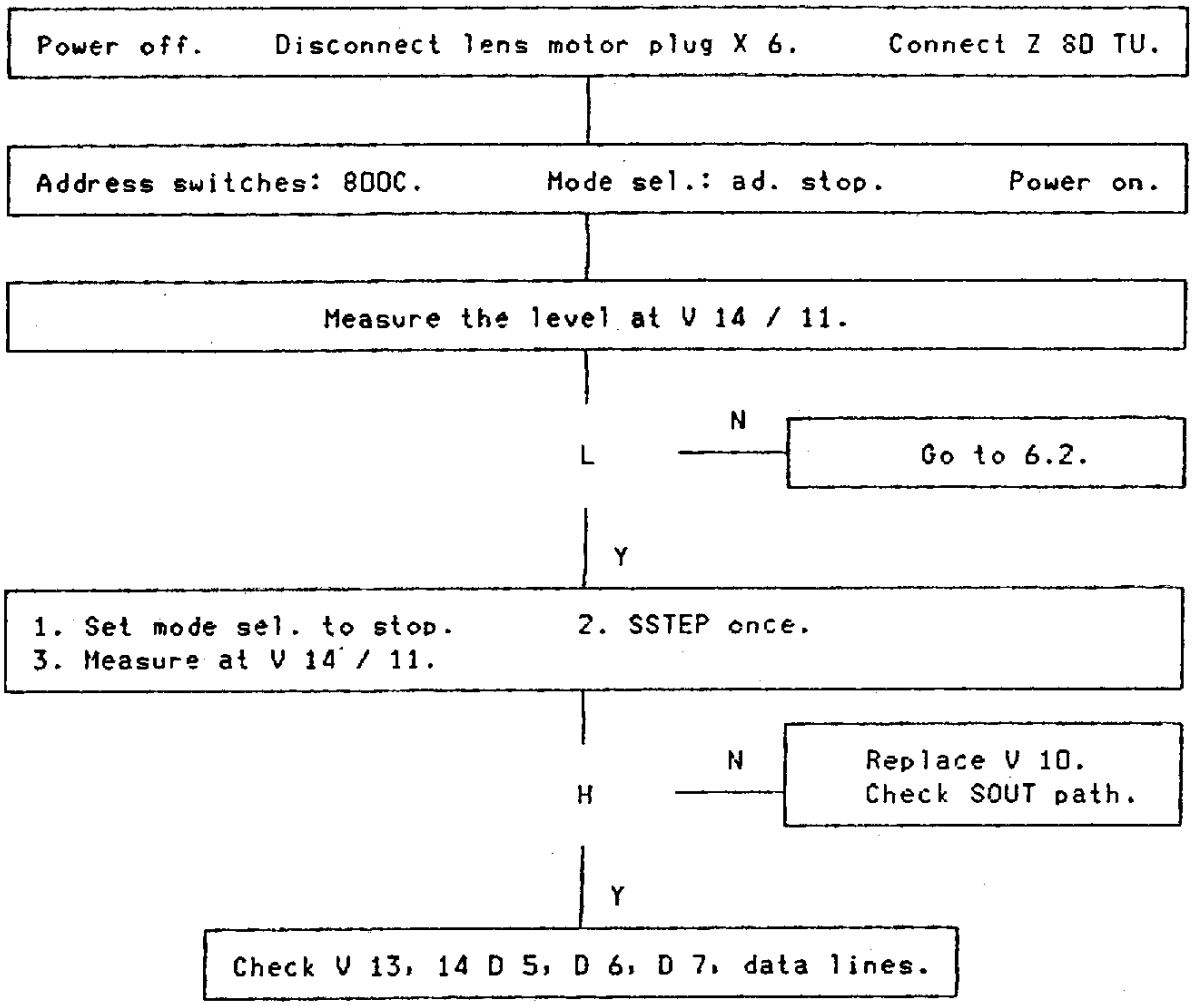

correct
N
Adjust R 25.
Y
Set the head to center position.
Press the "head up" key.
Measure the signals at V 23 / 5.
They must correspond to the signals at P 3.
correct
N
Check V 25.
Y
Press the "head down" key.
Measure the signal at V 23 / 13.
It must correspond to the signal at P 3.
correct
N
Check V 25.
Y
Press and hold the "head up" key.
Measure at P 4.
2 V
N
Adjust R 46.
Check V 24, V 10.
Y
Check V 23, 24, 10.

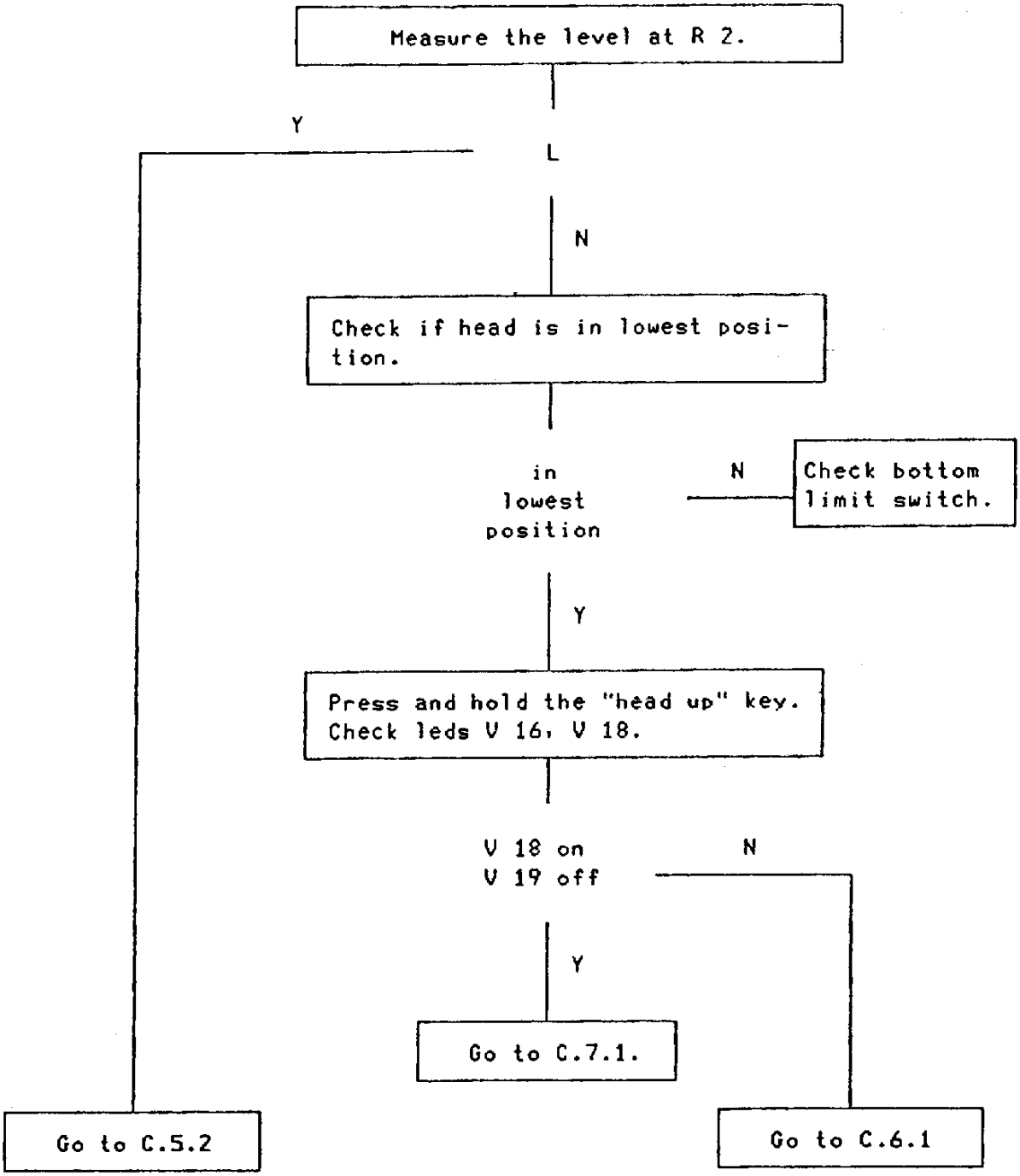
FAILURE CHART

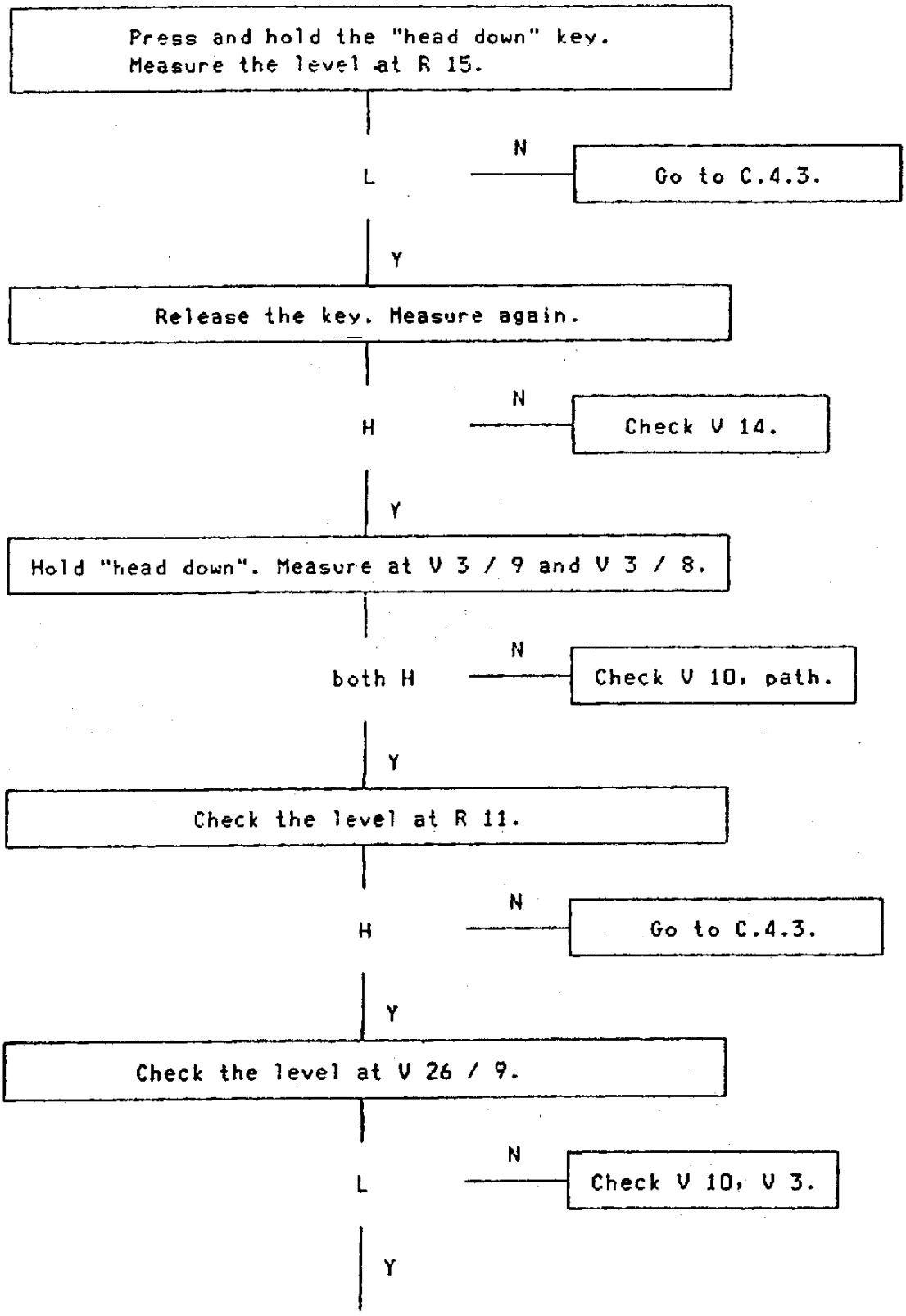


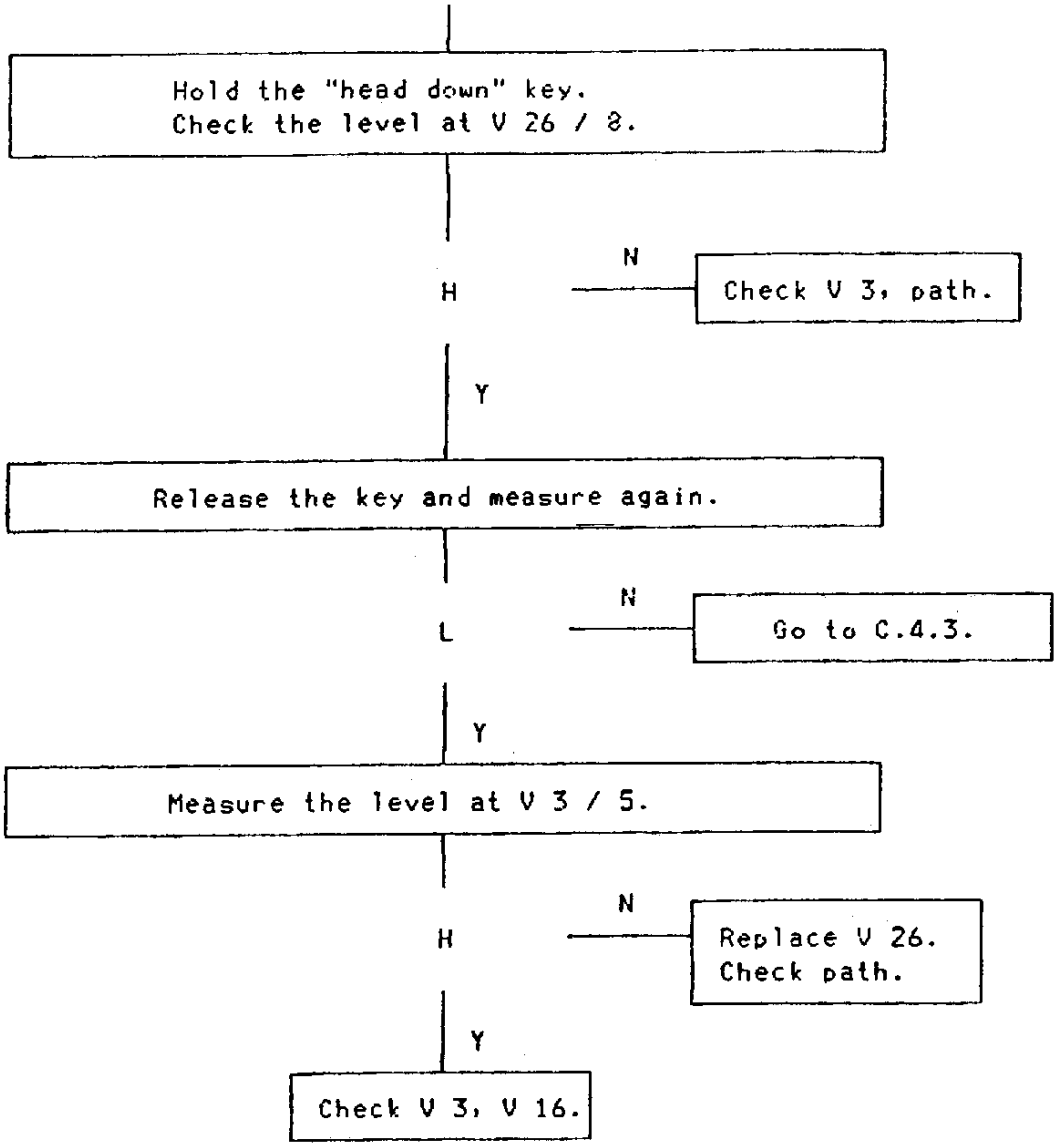

Press and hold the "head down" key.
V26/4 = L
N
Y
Check V 37, 38, R 55.
V17/11 = L
N
Check V 17.
Y
Check V 19, 26

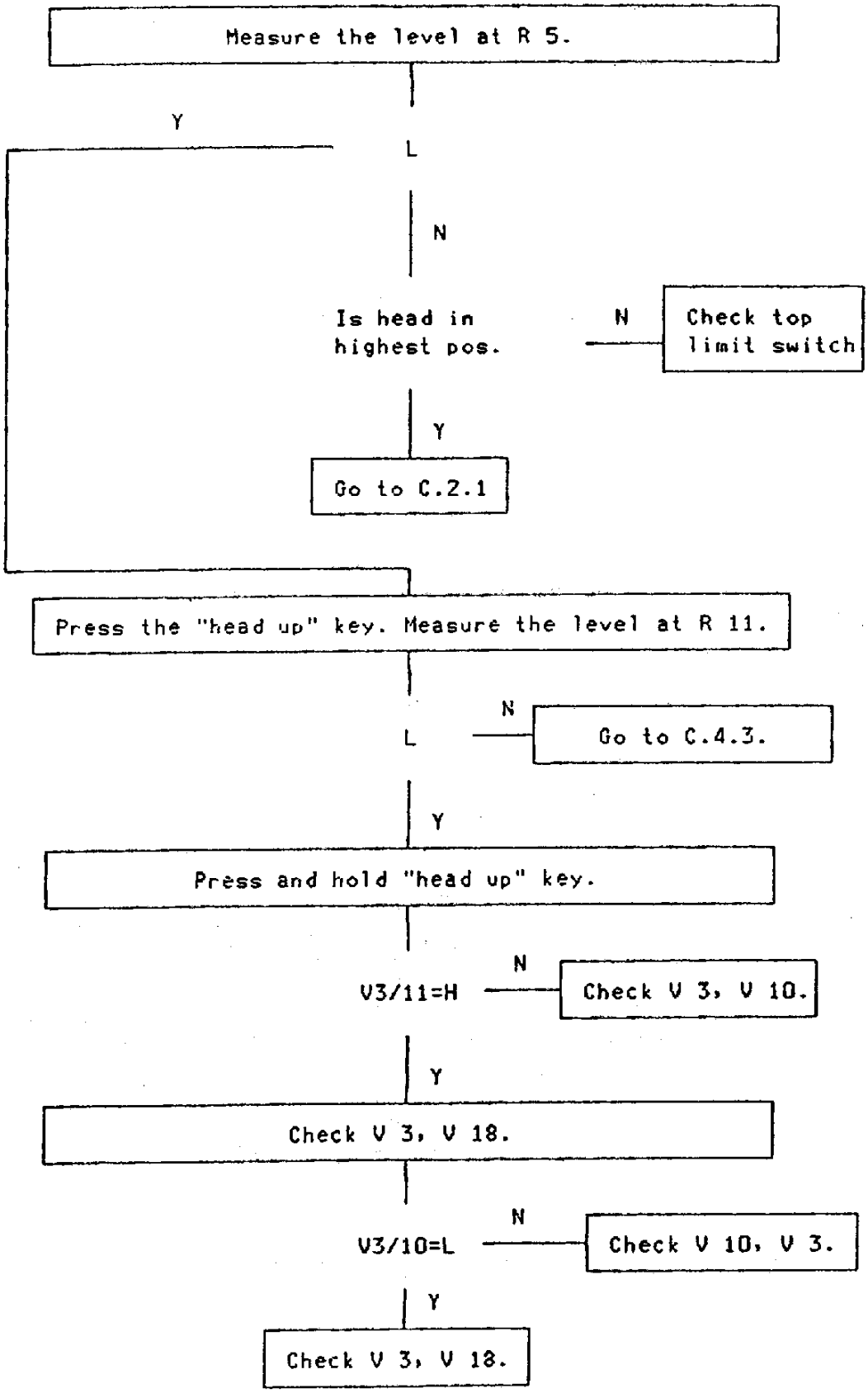

Press the indicated keys and measure at V 13 on the interface PCB.
Key
V 13 / pin
level
head up
14
12
9
L
H
L
head down
and rapid
14
12
9
H
L
H
correct
N
Go to C.4.4.
Y
Check V 2, V 4, V 6 on the head motor interface PCB.
Check connections, R 9, 10, 11.

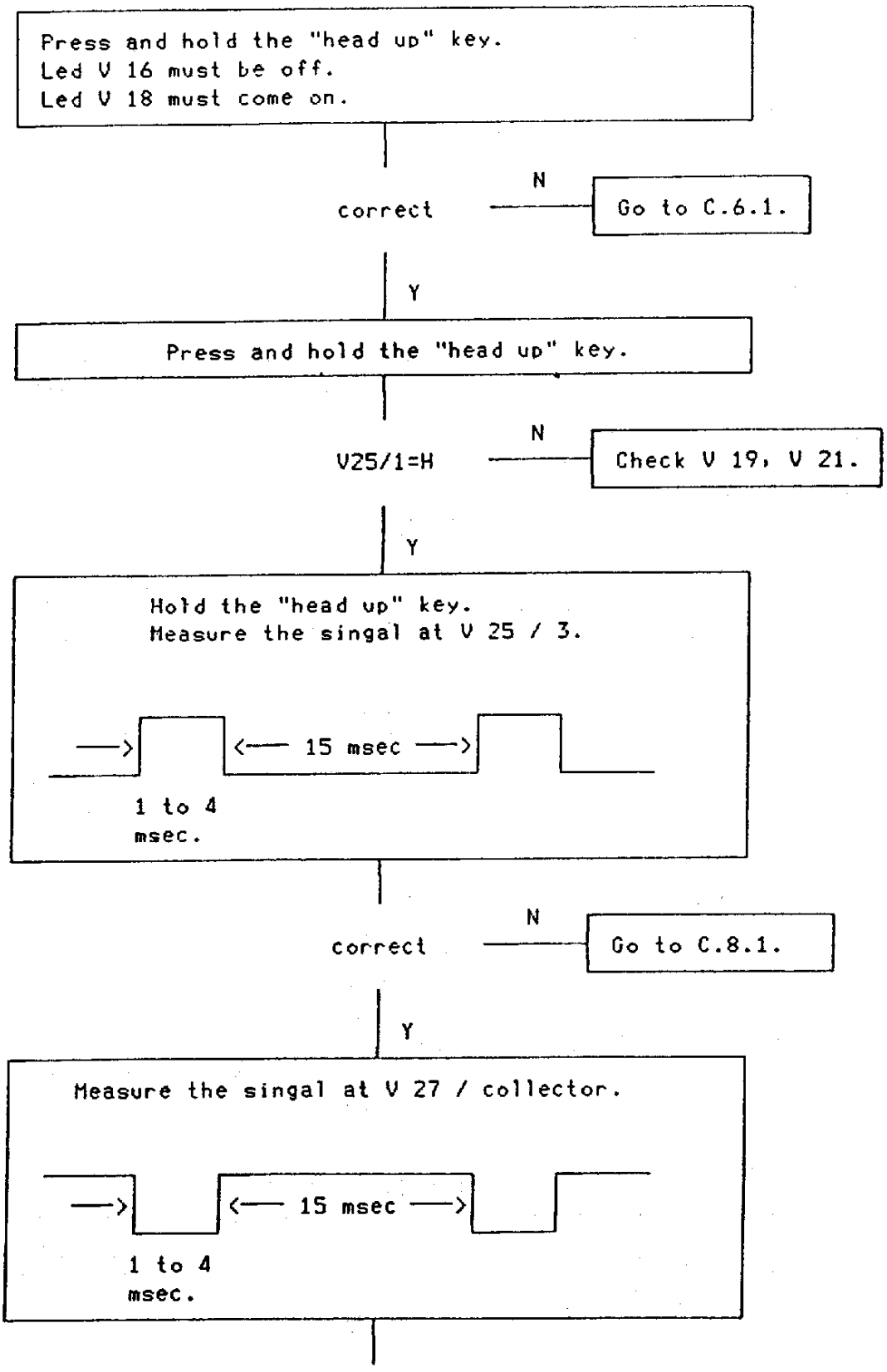

Power off. Disconnect lens motor plug X 6. Connect Z 80 TU.
Address switches: 800C. Mode sel.: ad. stop. Power on.
Measure the level at V 14 / 11.
L
N
Go to 6.2.
Y
1. Set mode sel. to stop. 2. SSTEP once.
3. Measure at V 14 / 11.
H
N
Replace V 10.
Check SOUT path.
Y
Check V 13, 14 D 5, D 6, D 7, data lines.

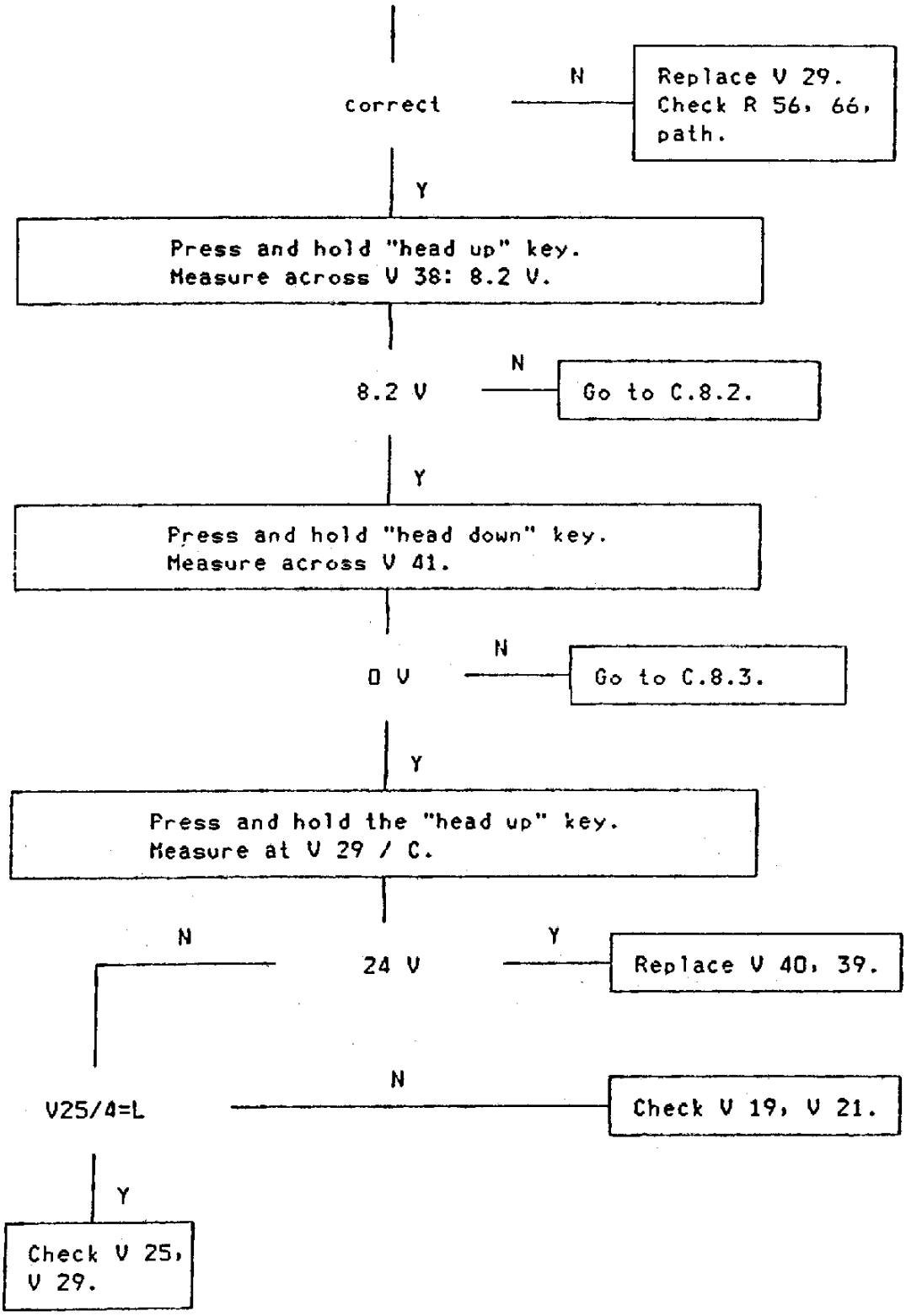

Measure the level at R 2.
Y
L
N
Check if head is in lowest position.
in lowest position
N
Check bottom limit switch.
Y
Press and hold the "head up" key.
Check leds V 16, V 18.
V 18 on
V 19 off
N
Y
Go to C.7.1.
Go to C.5.2
Go to C.6.1

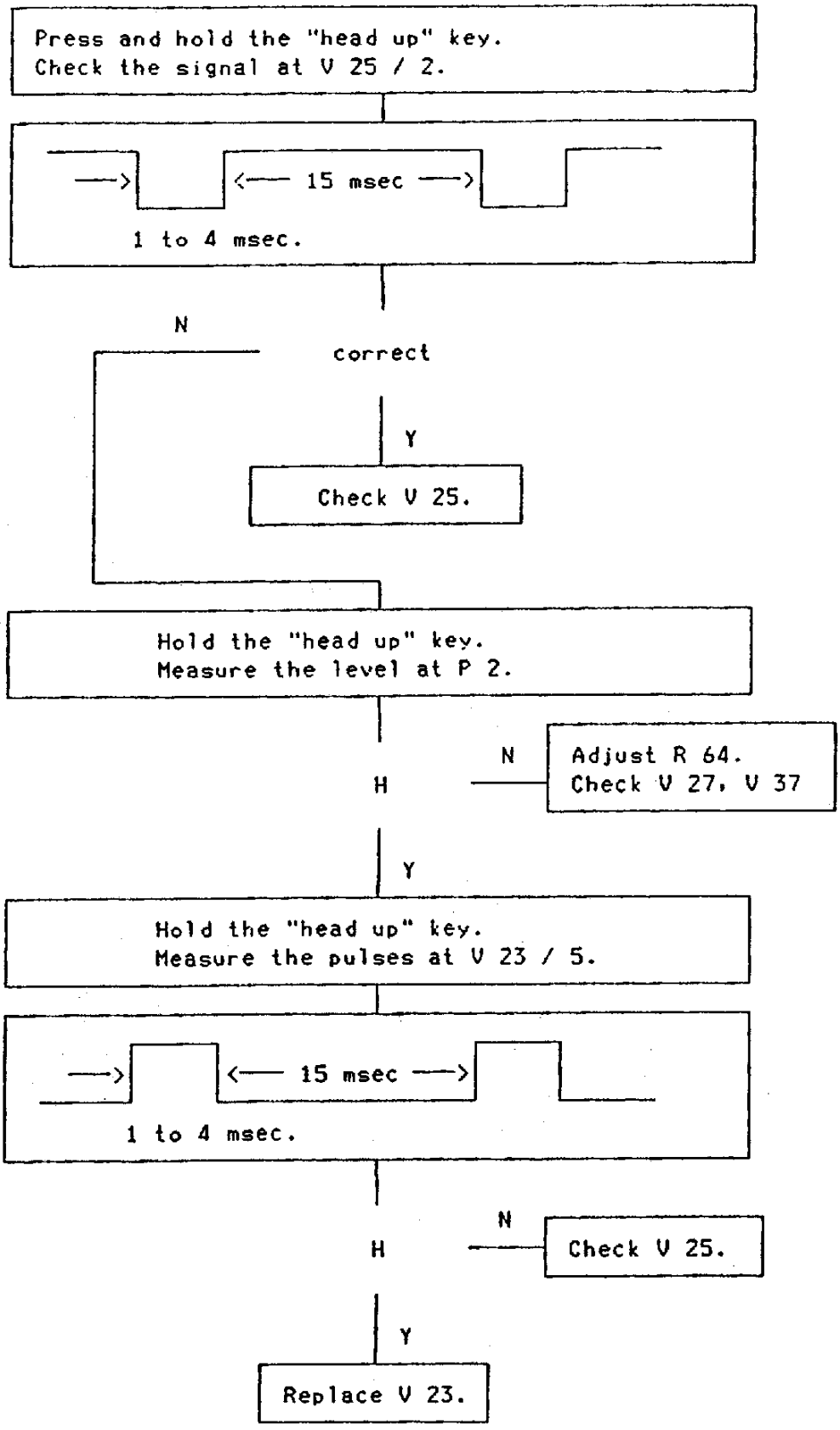

Press and hold the "head down" key.
Measure the level at R 15.
L
N
Go to C.4.3.
Y
Release the key. Measure again.
H
N
Check V 14.
Y
Hold "head down". Measure at V 3 / 9 and V 3 / 8.
both H
N
Check V 10, path.
Y
Check the level at R 11.
H
N
Go to C.4.3.
Y
Check the level at V 26 / 9.
L
N
Check V 10, V 3.
Y

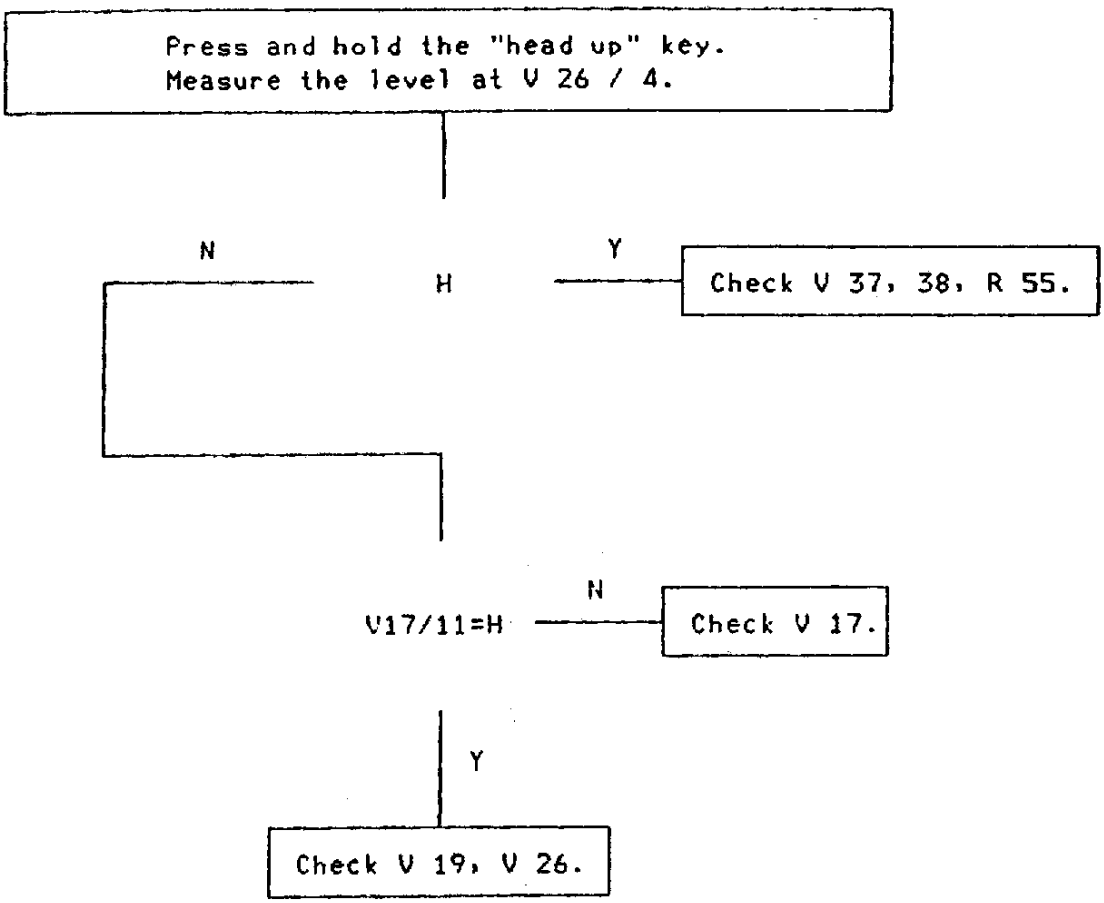

Hold the "head down" key.
Check the level at V 26 / 8.
H
N
Check V 3, path.
Y
Release the key and measure again.
L
N
Go to C.4.3.
Y
Measure the level at V 3 / 5.
H
N
Replace V 26.
Check path.
Y
Check V 3, V 16.

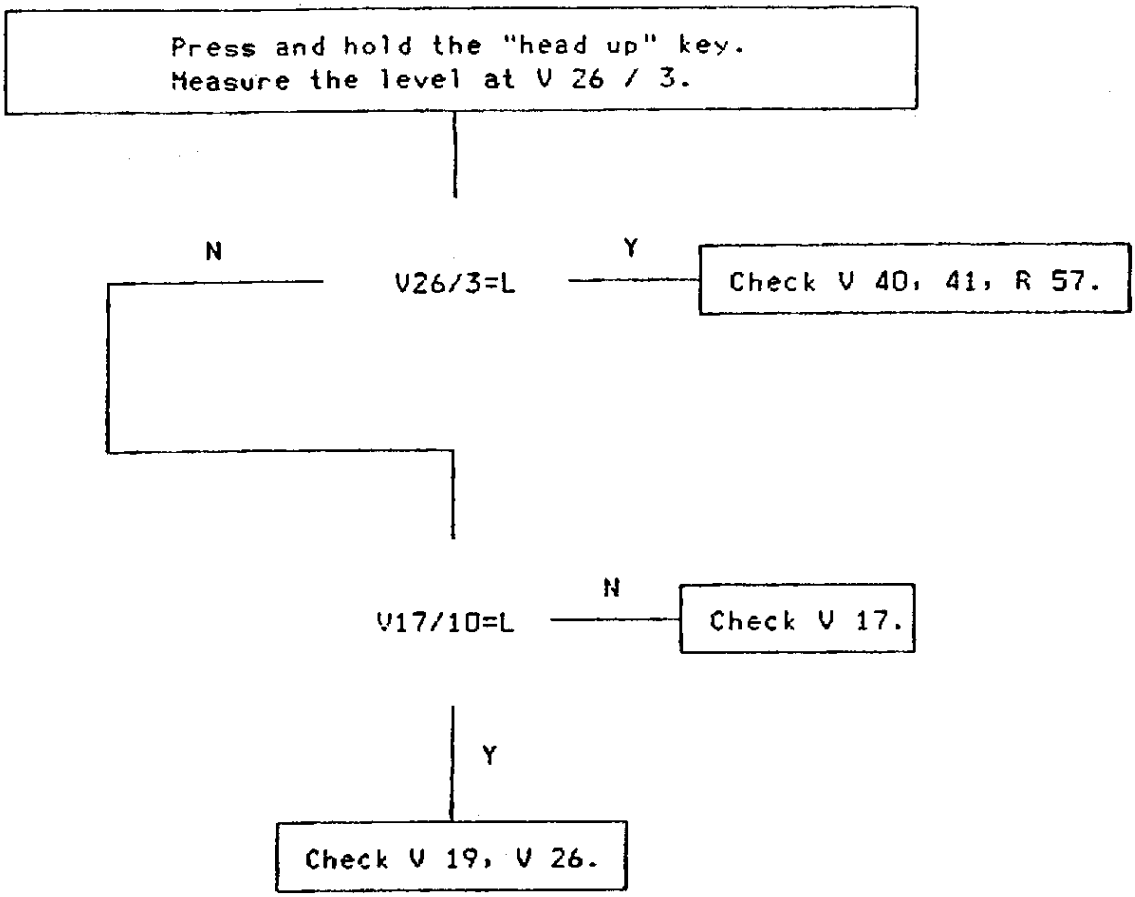

Measure the level at R 5.
Y
L
N
Is head in highest pos.
N
Check top limit switch
Y
Go to C.2.1
Press the "head up" key. Measure the level at R 11.
L
N
Go to C.4.3.
Y
Press and hold "head up" key.
V3/11=H
N
Check V 3, V 10.
Y
Check V 3, V 18.
V3/10=L
N
Check V 10, V 3.
Y
Check V 3, V 18.

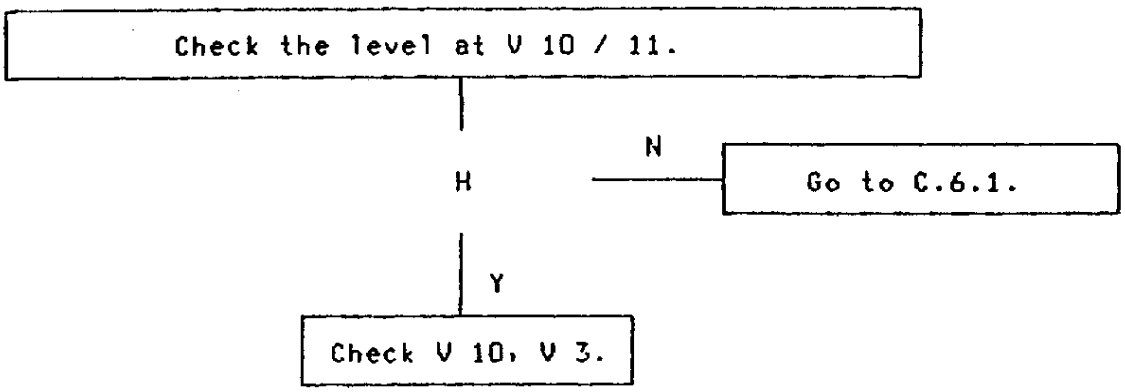

Press and hold the "head up" key.
Led V 16 must be off.
Led V 18 must come on.
correct
N
Go to C.6.1.
Y
Press and hold the "head up" key.
V25/1=H
N
Check V 19, V 21.
Y
Hold the "head up" key.
Measure the singal at V 25 / 3.
15 msec
1 to 4
msec.
correct
N
Go to C.8.1.
Y
Measure the singal at V 27 / collector.
15 msec
1 to 4
msec.

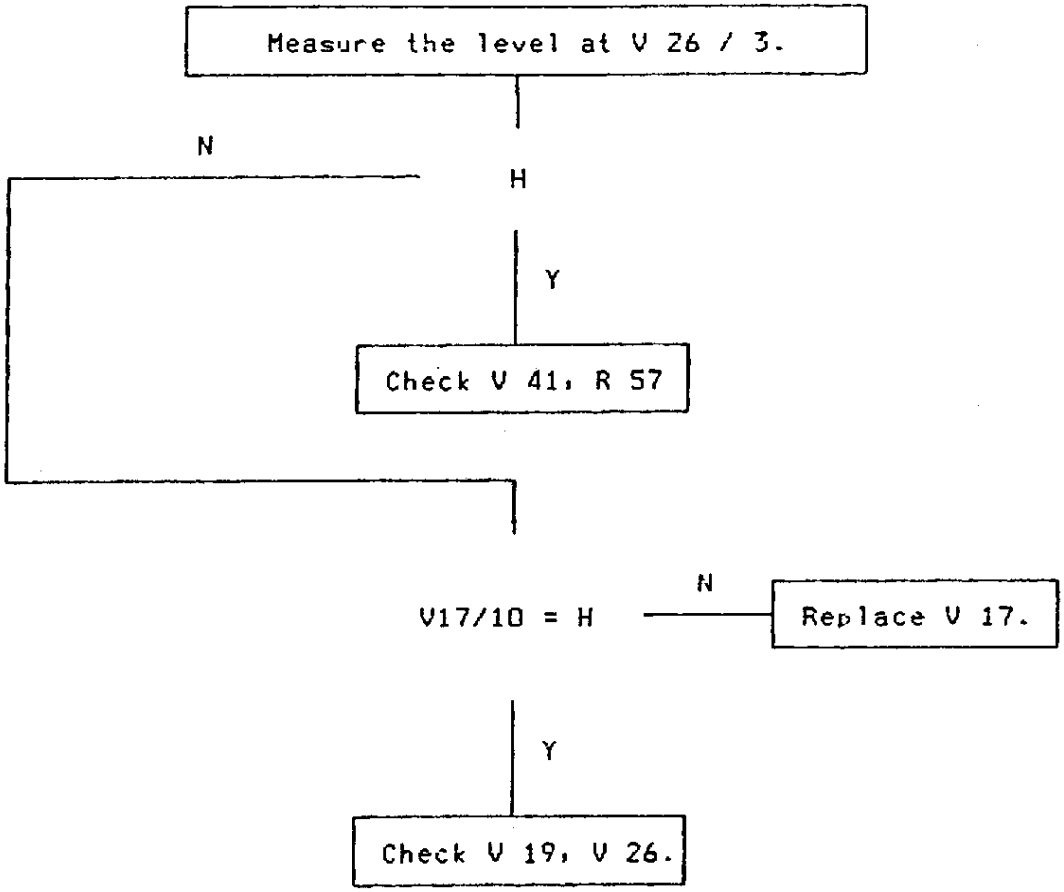

correct
N
Replace V 29.
Check R 56, 66,
path.
Y
Press and hold "head up" key.
Measure across V 38: 8.2 V.
8.2 V
N
Go to C.8.2.
Y
Press and hold "head down" key.
Measure across V 41.
0 V
N
Go to C.8.3.
Y
Press and hold the "head up" key.
Measure at V 29 / C.
N
24 V
Y
Replace V 40, 39.
V25/4=L
N
Check V 19, V 21.
Y
Check V 25,
V 29.

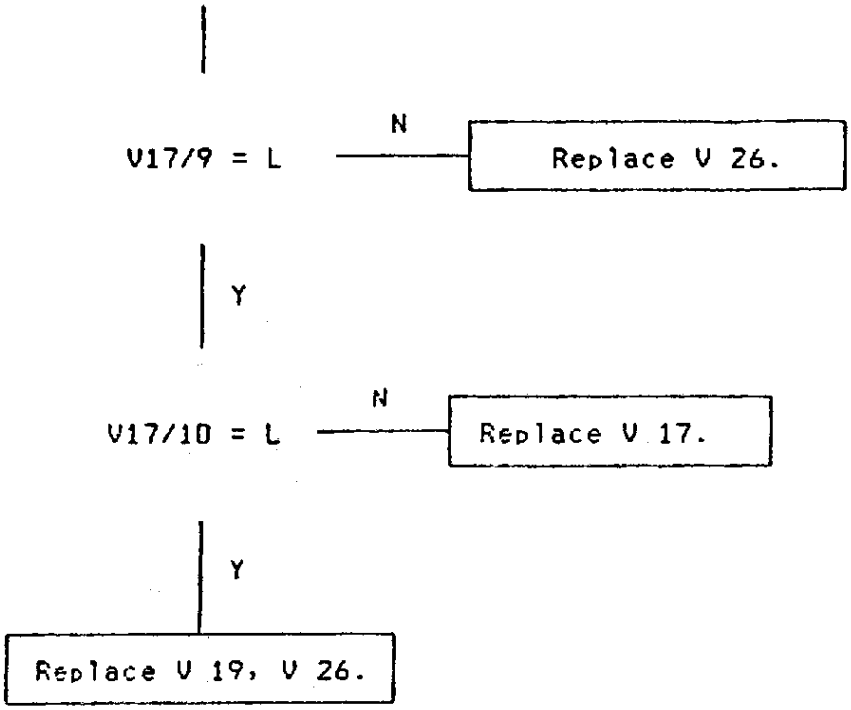

Press and hold the "head up" key.
Check the signal at V 25 / 2.
15 msec
1 to 4 msec.
N
correct
Y
Check V 25.
Hold the "head up" key.
Measure the level at P 2.
N
H
Adjust R 64.
Check V 27, V 37
Y
Hold the "head up" key.
Measure the pulses at V 23 / 5.
15 msec
1 to 4 msec.
N
H
Check V 25.
Y
Replace V 23.

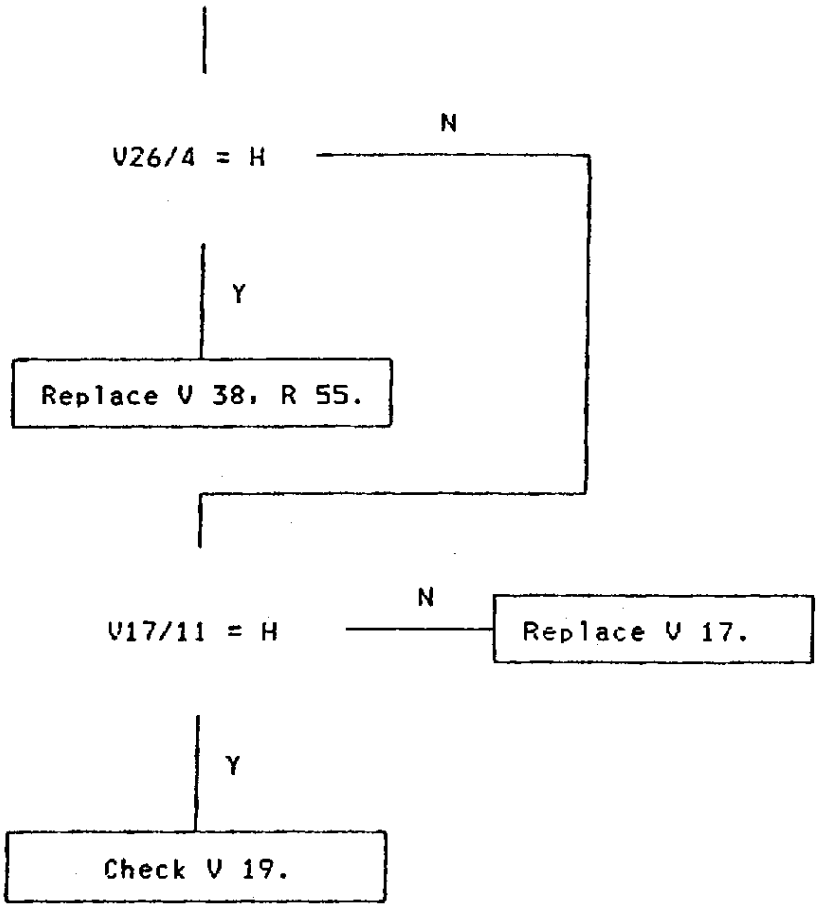

Press and hold the "head up" key.
Measure the level at V 26 / 4.
N
H
Y
Check V 37, 38, R 55.
V17/11=H
N
Check V 17.
Y
Check V 19, V 26.


Press and hold the "head up" key.
Measure the level at V 26 / 3.
N
V26/3=L
Y
Check V 40, 41, R 57.
V17/10=L
N
Check V 17.
Y
Check V 19, V 26.


Check the level at V 10 / 11.
N
H
Go to C.6.1.
Y
Check V 10, V 3.


Measure the level at V 26 / 3.
N
H
Y
Check V 41, R 57
V17/10 = H
N
Replace V 17.
Y
Check V 19, V 26.


V17/9 = L
N
Replace V 26.
Y
V17/10 = L
N
Replace V 17.
Y
Replace V 19, V 26.


V26/4 = H
N
Y
Replace V 38, R 55.
V17/11 = H
N
Replace V 17.
Y
Check V 19.

D.1 MOTOR CONTROL 24 VOLT PCB: FUNCTIONAL DESCRIPTION

DECODING STAGE

It consists of V 3, 10, 26.

The commands UP, DOWN and FAST are low active..

The inputs LIMIT SWITCH UP, DOWN are H active. The limit switches are closed when the head is not in the end position.

Thus, in the inactive state the limit switches connect these inputs to ground.

The and-gates V 3/c and d decode the inputs.

DOWN V 10/13	UP V 10/11	LIMIT SW. UP V 10/3	LIMIT SW. DOWN V 10/5	V 3/10	V 3/11
L	H	L	L	H	L
H	L	L	L	L	H
H	X	H	L	L	L
X	H	L	H	L	L
X	L	L	H	L	H
L	X	H	L	H	L

V 26/c is an EX-OR gate.

If both the up and down commands are active, output pin 10 goes to L level and stops the commands.

PULSE GENERATOR

Astable mulitvibrator V 20 produces pulses (pin 3) and a sawtooth (pin 6).

The sawtooth is compared to the feedback voltage available at V 24/1 via V 24/d.

The duty-cycle at V 10/2 is proportional to the feedback voltage.

Depending on the selected function (up or down), either V 25/3 or V 25/4 follows this frequency and switches transistor V 29 (V 27).

A larger load means a higher voltage at V 24/1 and a longer duty cycle at V 10/2.

In case the "fast" key is pressed, the pulses are suppressed via V 10/d and replaced by a steady H level. Thereby the motor receives full power instead of a pulsed signal.

V 24/c is a time delay circuit, to avoid a sudden voltage increase at the motor inputs.

LOAD FEEDBACK

In slow speed, the load condition is measured and translated into a proportional pulse to the power drivers.

Across R 53 (down) ar R 49 (up) the driving pulses are available.

Their amplitude decreases in case the motor load increases, as the voltage drop across R 68, 69 increases as well and less voltage reaches the motor.

The pulses charge C 19 via digital switches V 23/a (up) or V 23/b (down).

Capacitor C 19 charges up to a voltage proportional to the pulse amplitude.

At pin 7 of buffer V 24/b the same voltage appears.

V 24/a compares the desired speed (pin 3) to the feedback = actual speed.

The desired speed is adjusted via R 46.

The voltage available at V 24/1 is therefore proportional to the difference desired speed - actual speed.

Thru digital switches V 23/a, b the feedback is syncronized to the control pulses; monostable V 15 activates these switches to this purpose.

To achieve a high efficiency slow speed regulation, the motor speed is pulse-controlled.

The period of these pulses is sufficiently short to guarantee smooth motion.

The bridge configuration allows movement in both directions without the need of a dual supply voltage.

OVERLOAD PROTECTION

An electronic fuse protects motor and power stage from overload and short circuit condition.

The voltage drop across R 68, 69 is proportional to the motor load.

Part of this voltage drop reaches transistor V 36. If it exceeds 0.7 volts, V 36, 37 become conductive and trigger flip-flop V 21/c, d.

Pin 13 of V 24 is forced to L level. Consequently V 10/2 stays at L level and the driving transistors are disactivated.

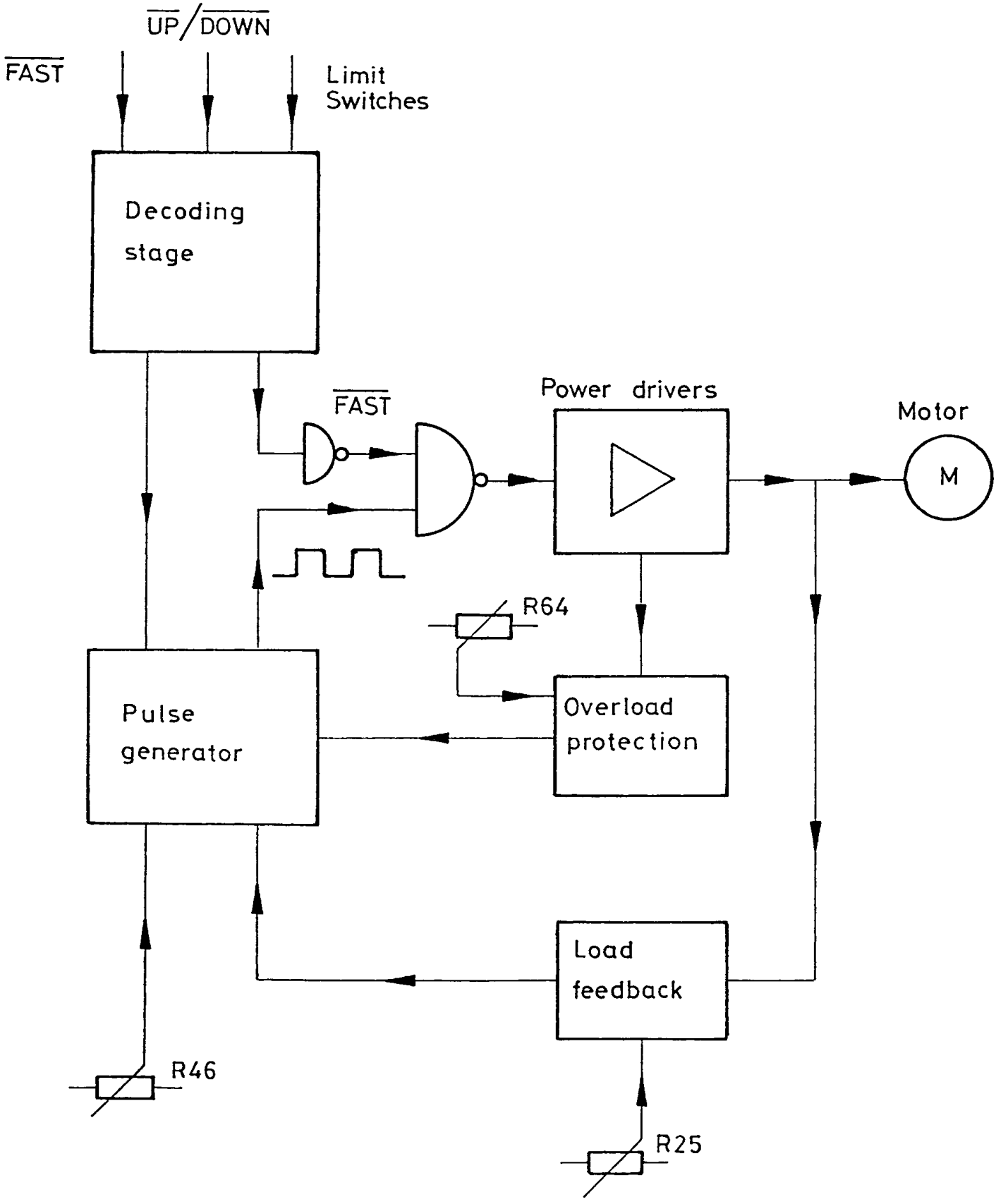
The motor current is interrupted.

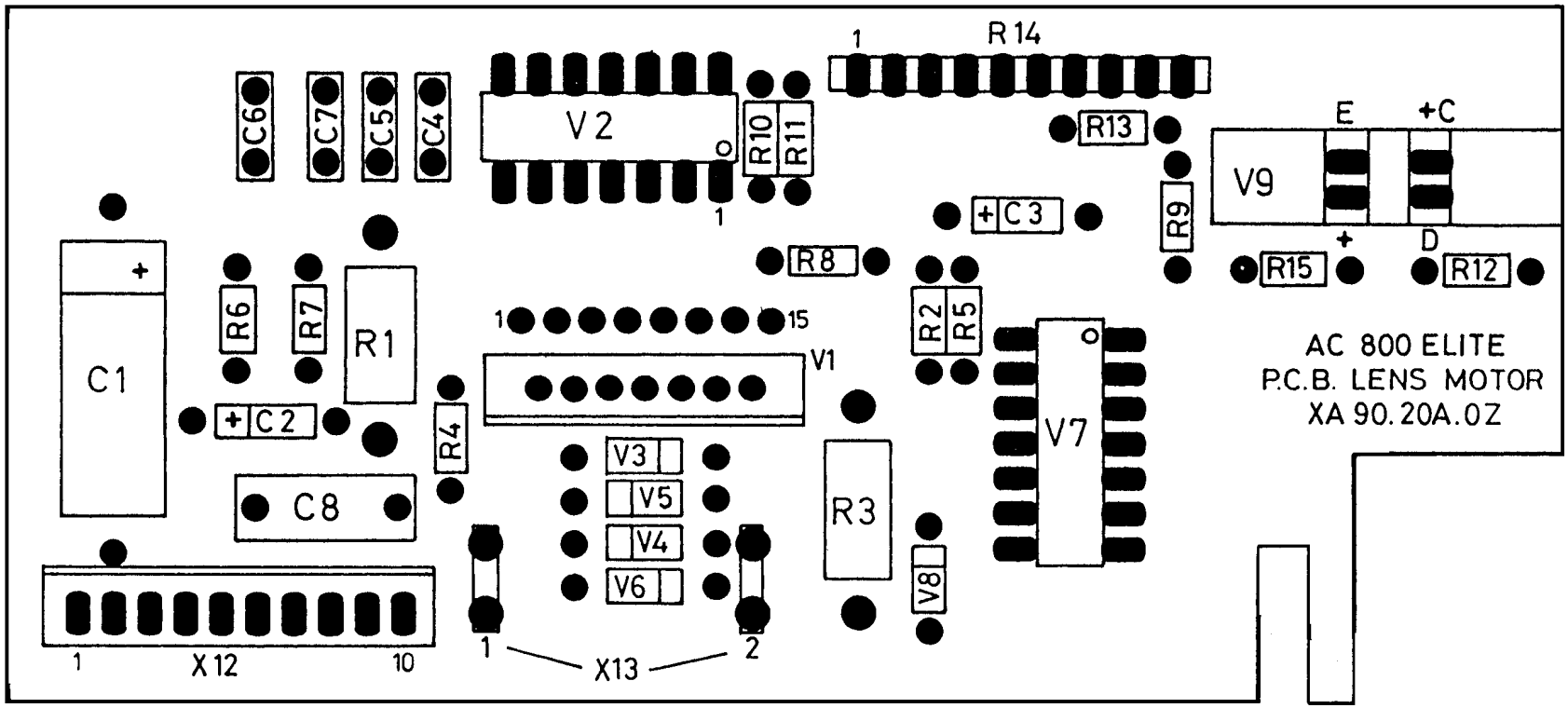
Flip-flop V 21 is reset by astable V 20.

If the short circuit condition persists, the flip-flop V 21 is set again.

Motor control 24 V

BLOCK DIAGRAM





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